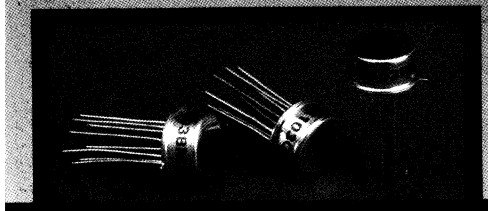
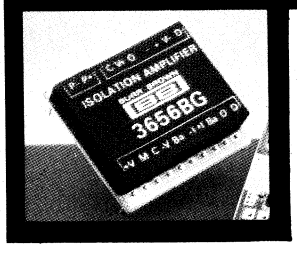
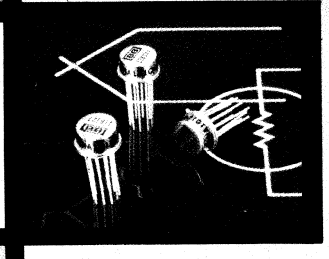
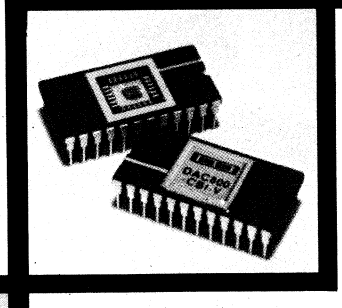
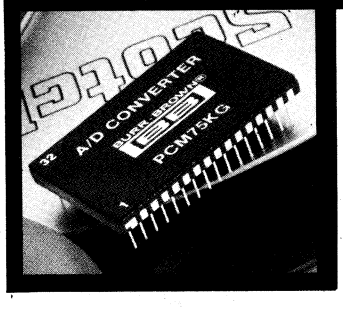
BURR-BROWN®











product data book supplement

MODEL INDEX

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

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SUPPLEMENT TO PRODUCT DATA BOOK

LI-288

Printed in U.S.A. August, 1983

INTRODUCTION

This supplement to the Burr-Brown Product Data Book contains product data sheets on new products that have been developed and introduced since the Data Book was published. Product lines such as Instrumentation and Isolation Amplifiers, Data Conversion and Acquisition, Microcomputer I/O Systems, Microterminals, Analog Circuit Functions, Power Supplies, and Fiber Optics are represented by these products.

The Model Index list on the inside of the front cover refers to models and page numbers in both the Product Data Book and this supplement. Products in this supplement are set in bold type.

A Selection Guide on page iii contains a summary of performance characteristics of all products in both the Product Data Book and this supplement.

A complete list of all Burr-Brown offices and sales representatives can be found on the inside of the back cover. If you have questions on any of our products please contact the nearest Burr-Brown office or sales representative.

SELECTION GUIDE

HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

Your requirements for precise, accurate op amp performance in critical applications dictate our product design direction. We have applied our unequalled skills and experience in op amp design (we marketed the first solid state op amp in 1959) to solve your problems when you must have special performance: *very low bias current, low noise, low voltage drift vs temperature, wide bandwidth, high voltage or high current.* This broad selection - offering special performance characteristics - lets you select the right op amp without compromising your design.

Each of these differing amplifier functions requires very specific expertise - in design, assembly and testing. We have developed a unique set of skills in each area and our complete microelectronic facilities fully support the challenge of meeting your most demanding needs.

GENERAL PURPOSE

These moderately priced FET and bipolar op amps offer good performance over a wide range of parameters. These are good options when a special function op amp is not required. You can be confident that Burr-Brown's quality and reliability are inherent in their design.

These give good performance over a wide range of parameters.

GENERAL PURPOSE														
		Offset Voltage		Bias	Open	Frequency Response		Rated Output						
Description	Model[1]	at 25°C ±mV max	Temp Drift ±μV/°C max	Current nA (25°C) max	Loop Gain dB, min	Unity Gain MHz	Slew Rate V/μsec	±V min	±mA min	Temp Range[2]	Package			Page
Bipolar	3500A	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99			1-62
	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99			1-62
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99			1-62
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99			1-62
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	MIL	TO-99			1-62
	3500T, (Q)	1	5	±15	93	1.5	1.0	10	10	MIL	TO-99			1-62
Military	3500/MIL Series	See Military Products, Page xvii												
Bipolar	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501C, (Q)	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501R	5	20	±15	93	0.5	0.1	10	5	MIL	TO-99			1-71
	3501S	2	10	±7	93	0.5	0.1	10	5	MIL	TO-99			1-71
Low Power	**OPA21A**	**0.1**	**1**	**25**	**120**	**0.3**	**0.2**	**13.7**	**1.4**	**MIL**	**TO-99/ DIP**			**1**
	OPA21B	**0.2**	**2**	**40**	**114**	**0.3**	**0.2**	**13.7**	**1.4**	**MIL**	**TO-99/ DIP**			**1**
	OPA21G	**0.5**	**5**	**50**	**114**	**0.3**	**0.2**	**13.6**	**1.3**	**Ind**	**TO-99/ DIP**			**1**
	OPA21E	**0.1**	**1**	**25**	**120**	**0.3**	**0.2**	**13.7**	**1.4**	**Ind**	**TO-99/ DIP**			**1**
	OPA21F	**0.2**	**2**	**40**	**114**	**0.3**	**0.2**	**13.7**	**1.4**	**Ind**	**TO-99/ DIP**			**1**
Switchable Input	**OPA201A**	**0.5**	**5**	**50**	**114**	**0.5[3]**	**0.1**	**13.5**	**5**	**Com**	**DIP**			**11**
	OPA201B	**0.2**	**2**	**40**	**114**	**0.5[3]**	**0.1**	**13.5**	**5**	**Com**	**DIP**			**11**
	OPA201C	**0.1**	**1**	**25**	**120**	**0.5[3]**	**0.1**	**13.5**	**5**	**Com**	**DIP**			**11**
	OPA201R	**0.5**	**5**	**50**	**114**	**0.5[3]**	**0.1**	**13.5**	**5**	**MIL**	**DIP**			**11**
	OPA201S	**0.2**	**2**	**40**	**114**	**0.5[3]**	**0.1**	**13.5**	**5**	**MIL**	**DIP**			**11**
FET	OPA103AM	0.50	25	−0.002	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103BM	0.50	15	−0.001	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103CM	0.25	5	−0.001	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103DM	0.25	2	−0.001	106	1	1.3	10	5	Ind	TO-99			1-36
	3542J, (Q)	20	50	−0.025	88	1.0	0.5	10	10	Com	TO-99			1-109
	3542S, (Q)	20	50	−0.025	88	1.0	0.5	10	10	MIL	TO-99			1-109
Wide Temp Range	OPA11HT	5	5[3]	±25	94	12.0	7.0	10	15	−55°C to +200°C	TO-99			1-8

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) Typical.

LOW NOISE

Now both FET and bipolar input op amps are offered with guaranteed low noise specifications. Until now the designer had to rely on "typical" specs for his demanding low noise designs. These fully characterized parts allow a truly complete error budget calculation.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

LOW NOISE														
Description	Model	Noise Voltage nV/√Hz at 10kHz max	Bias Current pA at 25°C max	Offset Voltage at 25°C mV max	Offset Voltage Temp Drift µV/°C max	Open Loop Gain dB min	Frequency Response GBW MHz	Frequency Response Slew Rate V/µsec min	Rated Output ±V min	Rated Output ±mA min	Temp Range(1)	Package		Page
OPA27 †A_{CL} > 1V/V	OPA27/37A, (/883)	3.8	±40k	0.025	0.6	120	8/40	1.7/11	10.0	17.6	MIL	TO-99, DIP		1-16
	OPA27/37B, (/883)	3.8	±55k	0.060	1.3	120	8/40	1.7/11	10.0	17.6	MIL	TO-99, DIP		1-16
OPA37 †A_{CL} > 5V/V	OPA27/37C, (/883)	4.5	±80k	0.100	1.8	97	8/40	1.7/11	10.0	17.6	MIL	TO-99, DIP		1-16
	OPA27/37E,	3.8	±40k	0.025	0.6	120	8/40	1.7/11	10.0	17.6	Ind	TO-99, DIP		1-16
	OPA27/37F,	3.8	±55k	0.060	1.3	120	8/40	1.7/11	10.0	17.6	Ind	TO-99, DIP		1-16
	OPA27/37G,	4.5	±80k	0.100	1.8	97	8/40	1.7/11	10.0	17.6	Ind	TO-99, DIP		1-16
†A_{CL} > 1V/V	OPA101AM	8	-15	±0.5	±10	94	20	5	12	12	Ind	TO-99		1-24
	OPA101BM	8	-10	±0.25	±5	94	20	5	12	12	Ind	TO-99		1-24
†A_{CL} > 3V/V	OPA102AM	8	-15	±0.5	±10	94	40	10	12	12	Ind	TO-99		1-24
	OPA102BM	8	-10	±0.25	±5	94	40	10	12	12	Ind	TO-99		1-24

†FET Input NOTES: 1) Ind = -25°C to +85°C; MIL = -55°C to +125°C.

LOW DRIFT

Low offset voltage drift vs temperature performance in both FET and bipolar input types is obtained by our sophisticated drift compensation techniques. First, the drift is measured and then special laser trim techniques used to minimize the drift and the initial offset voltage at 25°C. Finally, "max drift" performance is retested for conformance with specifications.

0.1µV/°C to 10µV/°C input offset voltage change with temperature.

LOW DRIFT														
Description	Model(1)	Offset Voltage at 25°C ±mV max	Offset Voltage Temp Drift ±µV/°C max	Bias Current nA 25°C max	Open Loop Gain dB, min	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/µsec	Rated Output ±V min	Rated Output ±mA min	Temp Range(2)	Package			Page
*Inverting Only	3291/14	0.02	0.10	±0.05	140	3	6	10	5	Ind	Module			1-52
	3292/14	0.05	0.30	±0.05	140	3	6	10	5	Ind	Module			1-52
	3293/14	0.10	1.0	±0.10	140	3	6	10	5	Ind	Module			1-52
FET	OPA103AM	0.50	25	-0.002	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103BM	0.50	15	-0.001	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103CM	0.25	5	-0.001	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103DM	0.25	2	-0.001	106	1	1.3	10	5	Ind	TO-99			1-36
Bipolar	OPA27/37A, (/883)	0.025	0.6	40	120	8/40(3)	2.8/17	10	17.6	MIL	TO-99, DIP			1-16
	OPA27/37B, (/883)	0.060	1.3	55	120	8/40(3)	2.8/17	10	17.6	MIL	TO-99, DIP			1-16
	OPA27/37C, (/883)	0.100	1.8	80	97	8/40(3)	2.8/17	10	17.6	MIL	TO-99, DIP			1-16
	OPA27/37E	0.025	0.6	40	120	8/40(3)	2.8/17	10	17.6	Ind	TO-99, DIP			1-16
	OPA27/37F	0.060	1.3	55	120	8/40(3)	2.8/17	10	17.6	Ind	TO-99, DIP			1-16
	OPA27/37G	0.100	1.8	80	97	8/40(3)	2.8/17	10	17.6	Ind	TO-99, DIP			1-16
	3510AM	0.15	2	±35	120	0.4	0.5	10	10	Ind	TO-99			1-83
	3510BM	0.12	1	±25	120	0.4	0.5	10	10	Ind	TO-99			1-83
	3510CM	0.06	0.5	±15	120	0.4	0.5	10	10	Ind	TO-99			1-83
Military	3510VM/MIL, /883B	See Military Products, **Page xvii**												
Bipolar	3500B	2	5	±20	93	1.5	0.8	10	10	Ind	TO-99			1-62
	3500C	1	3	±15	93	1.5	1.0	10	10	Ind	TO-99			1-62
	3500R, (Q)	5	20	±30	93	1.5	0.6	10	10	Ind	TO-99			1-62
	3500S, (Q)	2	10	±20	93	1.5	0.8	10	10	MIL	TO-99			1-62
	3500T, (Q)	1	3	±15	93	1.5	1.0	10	10	MIL	TO-99			1-62
	3500E	0.50	1	±50	100(5)	1.5	0.8	10	10	Ind	TO-99			1-62
	3500MP	0.20(4)	1(4)	±50	100(5)	1.5	0.8	10	10	Ind	TO-99			1-66
	3501A, (Q)	5	20	±15	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501B, (Q)	2	10	±7	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501C, (Q	2	5	±3	93	0.5	0.1	10	5	Ind	TO-99			1-71
	3501R	5	20	±15	93	0.5	0.1	10	5	MIL	TO-99			1-71
	3501S	2	10	±7	93	0.5	0.1	10	5	MIL	TO-99			1-71
High Voltage	3271/25	0.05	1.0	±0.08	140	1	20	110	20	Ind	Module			1-50

*Chopper-stabilized

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) Gain-bandwidth product for OPA37. 4) These specifications apply to the match between two devices. The 3500MP is a matched pair of amplifiers. 5) Typical.

LOW BIAS CURRENT

Our many years of experience in designing, manufacturing and testing FET amplifiers gives us unique abilities in providing low and ultra low bias current op amps. These amplifiers offer bias currents as low as 75fA (75×10^{-15} amps) and low voltage drift as low as 2μV/°C. With offset voltage laser-trimmed to as low as 250μV, the need for expensive trim pot adjustments is eliminated.

0.01pA to 1nA bias current

LOW BIAS CURRENT

Description	Model[1]	Offset Voltage at 25°C ±mV max	Offset Voltage Temp Drift ±V/°C max	Bias Current pA (25°C) max	Open Loop Gain dB, min	Frequency Response Unity Gain MHz	Frequency Response Slew Rate V/μsec	Rated Output ±V min	Rated Output ±mA min	Temp Range[2]	Package			Page
Low Drift	OPA103AM	0.50	25	−2	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103BM	0.50	15	−1	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103CM	0.25	5	−1	106	1	1.3	10	5	Ind	TO-99			1-36
	OPA103DM	0.25	2	−1	106	1	1.3	10	5	Ind	TO-99			1-36
Low Noise	OPA101AM	0.50	10	−15	94	10	6.5	12	12	Ind	TO-99			1-24
	OPA101BM	0.25	5	−10	94	10	6.5	12	12	Ind	TO-99			1-24
	OPA102AM	0.50	10	−15	94	40[3]	14	12	12	Ind	TO-99			1-24
	OPA102BM	0.25	5	−10	94	40[3]	14	12	12	Ind	TO-99			1-24
Ultra-Low Bias Current	OPA104AM	1.0	25	−0.300	106	1	2.2	10	5	Ind	TO-99			1-40
	OPA104BM	0.50	15	−0.150	106	1	2.2	10	5	Ind	TO-99			1-40
	OPA104CM	0.50	10	−0.075	106	1	2.2	10	5	Ind	TO-99			1-40
	3528AM, (Q)	0.50	15	−0.300	88	0.7	0.3	10	5	Ind	TO-99			1-103
	3528BM, (Q)	0.25	5	−0.150	92	0.7	0.3	10	5	Ind	TO-99			1-103
	3528CM, (Q)	0.50	10	−0.075	90	0.7	0.3	10	5	Ind	TO-99			1-103
	3523J, (Q)	1.0	50	−0.50	100	1	0.6	10	10	Com	TO-99			1-95
	3523K	0.50	25	−0.25	100	1	0.6	10	10	Com	TO-99			1-95
	3523L, (Q)	0.50	25	−0.10	100	1	0.6	10	10	Com	TO-99			1-95
Inverting Only	3430J	Adj. to 0	30	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module			1-60
	3430K	Adj. to 0	10	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module			1-60
Noninverting Only	3431J	Adj. to 0	30	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module			1-60
	3431K	Adj. to 0	10	±0.01	100	2kHz	0.4V/msec	10	5	Com	Module			1-60
Low Cost	**OPA100AM**	**1**	**15**	**±3**	**94**	**1**	**2**	**10**	**5**	**Ind**	**TO-99**			**5**
	OPA100BM	**0.5**	**10**	**±2**	**100**	**1**	**2**	**10**	**5**	**Ind**	**TO-99**			**5**
	OPA100CM	**0.25**	**5**	**±1**	**106**	**1**	**2**	**10**	**5**	**Ind**	**TO-99**			**5**
	OPA100SM	**0.5**	**10**	**±2**	**100**	**1**	**2**	**10**	**5**	**MIL**	**TO-99**			**5**
	3542J	20	50	−25	88	1	0.5	10	10	Com	TO-99			1-109
	3542S	20	50	−25	88	1	0.5	10	10	MIL	TO-99			1-109
Chopper-Stabilized	3291/14	0.02	0.1	±50	140	3	6	10	5	Ind	Module			1-52
	3292/14	0.05	0.3	±50	140	3	6	10	5	Ind	Module			1-52
	3293/14	0.10	1	±100	140	3	6	10	5	Ind	Module			1-52
	3271/25	0.05	1	±80	140	1	20	110	20	Ind	Module			1-50
Wideband	3554AM, (Q)	2	50	−50	100	1000[3]	1000	10	100	Ind	TO-3			1-125
	3554BM, (Q)	1	15	−50	100	1000[3]	1000	10	100	Ind	TO-3			1-125
	3554SM, (Q)	1	25	−50	100	1000[3]	1000	10	100	MIL	TO-3			1-125
Buffer	3553AM, (Q)	50	300	−200	NA	300[4]	2000	10	200	Ind	TO-3			1-123
High Current	3571AM, (Q)	2	40	−100	94	0.5	3	30	1A	Ind	TO-3			1-133
	3572AM	2	40	−100	94	0.5	3	30	2A	Ind	TO-3			1-133
High Voltage	3580J	10	30	−50	86	5	15	30	60	Com	TO-3			1-143
	3581J	3	25	−20	94	5	20	70	30	Com	TO-3			1-143
	3582J, (Q)	3	25	−20	100	5	20	145	15	Com	TO-3			1-143
	3583AM, (Q)	3	25	−20	105	5	30	140	75	Ind	TO-3			1-147
	3583JM	3	25	−20	94	5	30	140	75	Com	TO-3			1-147
	3584JM, (Q)	3	25	−20	100	20[3]	150	145	15	Com	TO-3			1-147
General Purpose	3522J	1.0	50	−10	94	1	0.6	10	10	Com	TO-99			1-89
	3522K	0.50	10	−5	94	1	0.6	10	10	Com	TO-99			1-89
	3522L	0.50	25	−1	94	1	0.6	10	10	Com	TO-99			1-89
	3522S, (Q)	0.50	25	−5	94	1	0.6	10	10	MIL	TO-99			1-89
Ultra-low Drift	3527AM, (Q)	0.50	10	−5	100	1	0.6	10	10	Ind	TO-99			1-99
	3527BM, (Q)	0.25	5	−2	100	1	0.6	10	10	Ind	TO-99			1-99
	3527CM, (Q)	0.25	2	−5	100	1	0.6	10	10	Ind	TO-99			1-99
	3521H	0.50	10	−20	94	1.5	0.6	10	10	Com	TO-99			1-89
	3521J, (Q)	0.25	5	−20	94	1.5	0.6	10	10	Com	TO-99			1-89
	3521K	0.25	2	−15	94	1.5	0.6	10	10	Com	TO-99			1-89
	3521L	0.25	1	−10	94	1.5	0.6	10	10	Com	TO-99			1-89
	3521R, (Q)	0.25	5	−20	94	1.5	0.6	10	10	MIL	TO-99			1-89

NOTES: (1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) Gain-bandwidth product. 4) −3dB bandwidth.

WIDE BANDWIDTH

Design expertise in wideband circuits combines with our fully developed hybrid technology to create cost effective wideband op amps. Hybrid IC performance - in bandwidth, settling time and output current - cannot be duplicated in less expensive monolithic designs.

WIDE BANDWIDTH														
		Frequency Response				Rated Output		Offset Voltage		Open Loop				
Description	Model[1]	GBW MHz	Slew Rate V/μsec min	t_s ±0.1% nsec	Compensation	±V min	±mA min	at 25°C ±mV max	Temp Drift ±μV/°C max	Gain dB	Temp Range[2]	Package		Page
Differential	3554AM, (Q)	1700, A = 1000	1000	120	ext.	10	100	2	50	100	Ind	TO-3		1-125
	3554BM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	15	100	Ind	TO-3		1-125
	3554SM, (Q)	1700, A = 1000	1000	120	ext.	10	100	1	25	100	MIL	TO-3		1-125
	3551J	50, A = 10	250	400	ext.	10	10	1	50[3]	100	Com	TO-99		1-117
	3551S, (Q)	50, A = 10	250	400	ext.	10	10	1	50[3]	100	MIL	TO-99		1-117
	3550J	10, A = 1	65	400	int.	10	10	1	50[3]	100	Com	TO-99		1-113
	3550K	20, A = 1	100	400	int.	10	10	1	50[3]	100	Com	TO-99		1-113
	3550S, (Q)	10, A = 1	65	400	int.	10	10	1	50[3]	100	MIL	TO-99		1-113
	3508J	100, A = 100	20	--	ext.	10	10	5	30[3]	103	Com	TO-99		1-79
	3507J, (Q)	20, A = 10	80	200	ext.	10	10	10	30[3]	83	Com	TO-99		1-75
	OPA605H/A	200, A = 1000	300[3]	300	ext.	10	30	1	25	96	Com/Ind	DIP		1-44
	OPA605J/B	200, A = 1000	300[3]	300	ext.	10	30	0.5	10	96	Com/Ind	DIP		1-44
	OPA605K/C	200, A = 1000	300[3]	300	ext.	10	30	0.5	5	96	Com/Ind	DIP		1-44
	OPA27/37A	8/40	1.7/11	--	int[4]	10	16	0.025	0.6	120	MIL	TO-99, DIP		1-16
	OPA27/37B	8/40	1.7/11	--	int[4]	10	16	0.060	1.3	120	MIL	TO-99, DIP		1-16
	OPA27/37C	8/40	1.7/11	--	int[4]	10	16	0.100	1.8	97	MIL	TO-99, DIP		1-16
	OPA27/37E	8/40	1.7/11	--	int[4]	10	16	0.025	0.6	120	Ind	TO-99, DIP		1-16
	OPA27/37F	8/40	1.7/11	--	int[4]	10	16	0.060	1.3	120	Ind	TO-99, DIP		1-16
	OPA27/37G	8/40	1.7/11	--	int[4]	10	16	0.100	1.8	97	Ind	TO-99, DIP		1-16
Low Noise	OPA101AM	20, A = 100	5	2.5	int.	12	12	0.5	10	105	Ind	TO-99		1-24
	OPA101BM	20, A = 100	5	2.5	int.	12	12	0.25	5	105	Ind	TO-99		1-24
	OPA102AM	40, A = 100	10	1.5	int.	12	12	0.5	10	105	Ind	TO-99		1-24
	OPA102BM	40, A = 100	10	1.5	int.	12	12	0.25	5	105	Ind	TO-99		1-24
Military	OPA600/MIL Series	See Military Products, Page xvii												
Unity-Gain Buffer	3553AM, (Q)	32	2000	--	--	10	200	50	300[3]	NA	Ind	TO-3		1-121
Wide Temp	OPA11HT	12, A = 1	4	1500	int.	10	15	5[3]	5	98	+175°C	TO-99		1-8
	OPA12HT	20, A = 10	80	200	ext.	10	10	10	30[3]	83	+175°C	TO-99		1-12

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) Typical. 4) G = 5 min for OPA37.

HIGH VOLTAGE - HIGH CURRENT

These IC op amp designs set the pace for the industry and are a product of our extensive hybrid circuit technology. Output currents up to ±5A peak and voltages up to ±145V are available.

Output voltages > ±10V to ±145V.

HIGH VOLTAGE														
		Rated Output		Offset Voltage		Bias Current	Frequency Response		Open Loop					
Description	Model[1]	±V min	±mA min	at 25°C ±mV max	Temp Drift ±μV/°C max	pA (25°C) max	Unity-Gain MHz	Slew Rate V/μsec	Gain dB	Temp Range[2]	Package			Page
FET	3584JM, (Q)	145	15	3	25	−20	20[3]	150	120	Com	TO-3			1-51
	3583AM, (Q)	140	75	3	25	−20	5	30	118	Ind	TO-3			1-147
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3			1-147
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3			1-143
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3			1-143
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3			1-143
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3			1-133
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3			1-133
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3			1-139
Chopper-Stabilized	3271/25	110	20	0.05	1	±80	1	20	140	Ind	Module			1-50

Output currents > ±15mA to ±10A.

HIGH CURRENT													
		Rated Output		Offset Voltage		Bias Current	Frequency Response		Open Loop Gain	Temp Range[2]	Package			
				at 25°C	Temp Drift									
Description	Model[1]	±V min	±mA min	±mV max	±μV/°C max	pA (25°C) max	Unity-Gain MHz	Slew Rate V/μsec	dB					Page
High Power	**OPA501AM**	**20**	**10A**	**10**	**65**	**40nA**	**1**	**1.5**	**94**	**Ind**	**TO-3**			**19**
	OPA501BM	**26**	**10A**	**5**	**40**	**20nA**	**1**	**1.5**	**98**	**Ind**	**TO-3**			**19**
	OPA501RM	**20**	**10A**	**10**	**65**	**40nA**	**1**	**1.5**	**94**	**MIL**	**TO-3**			**19**
	OPA501SM	**26**	**10A**	**5**	**40**	**20nA**	**1**	**1.5**	**98**	**MIL**	**TO-3**			**19**
	3573AM	20	2A[5]	10	65	40nA	1	2.6	94	Ind	TO-3			1-139
	3572AM	30	2A[5]	2	40	−100	0.5	3	94	Ind	TO-3			1-133
	3571AM, (Q)	30	1A[4]	2	40	−100	0.5	3	94	Ind	TO-3			1-133
Wideband	3554AM, (Q)	10	100	2	50	−50	1700[3]	1200	100	Ind	TO-3			1-125
	3554BM, (Q)	10	100	1	15	−50	1700[3]	1200	100	Ind	TO-3			1-125
	3554SM, (Q)	10	100	1	25	−50	1700[3]	1200	100	MIL	TO-3			1-125
High Voltage	3584JM, (Q)	145	15	3	25	−20	20[3]	150	126	Com	TO-3			1-151
	3583AM	140	75	3	25	−20	5	30	118	Ind	TO-3			1-147
	3583JM	140	75	3	25	−20	5	30	118	Com	TO-3			1-147
	3582J	145	15	3	25	−20	5	20	118	Com	TO-3			1-143
	3581J	70	30	3	25	−20	5	20	112	Com	TO-3			1-143
	3580J	30	60	10	30	−50	5	15	106	Com	TO-3			1-143
Booster (Buffer)	3553AM, (Q)	10	200	50	300[6]	−200	300	2000	NA	Ind	TO-3			1-121
	3329/03	10	100	50	--	Bipolar	5	--	NA	Ind	DIP			1-58

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) Gain-bandwidth product. 4) 2A peak. 5) 5A peak. 6) Typical.

UNITY-GAIN BUFFER (Power Booster)

These versatile amplifiers: boost the output current capability of another amplifier; buffer an impedance that might load a critical circuit; may be used inside the feedback loop of another op amp to form a current-boosted, composite amplifier. Currents as high as ±100mA are available with speeds of 2000V/sec.

UNITY-GAIN BUFFER														
		Rated Output		Frequency Response					Open Loop Gain					
		±V	±mA	-3dB	Full Pwr BW	Slew Rate	Gain	Input Impedance		Temp Range[1]	Package			
Description	Model	min	min	MHz	MHz	V/μsec	V/V	Ω	dB					Page
Noninverting	3553AM	10	200	300	32	2000	≈ 1	10^{11}	NA	Ind	TO-3			1-121
	3329/03	10	100	5	1	--	≈ 1	10k	NA	Ind	DIP			1-58

NOTES: 1) Ind = −25°C to +85°C.

INSTRUMENTATION AMPLIFIERS AND PROGRAMMABLE GAIN AMPLIFIERS

INSTRUMENTATION AMPLIFIERS

Performance requirements for instrumentation amplifiers call on different talents - in design, manufacturing and testing - than those associated with producing simpler operational amplifers. We have perfected our thin-film resistor technology, an essential factor in achieving excellent matching and tracking of the critical resistors in the amplifier's circuit. Laser-trimmed to produce the high accuracy demanded by you, these thin-film resistor networks provide excellent performance and stability at low cost.

What is an instrumentation amplifier? It's a closed-loop, differential input gain block. The primary function of this committed circuit is to accurately amplify the voltage applied to its inputs. An instrumentation amplifier responds only to the difference between the two input signals. It exhibits extremely high impedance between the two input terminals and from each terminal to ground. The output voltage produced is single-ended with respect to ground and is equal to the product of amplifier gain and the difference of the two input voltages.

Where are instrumentation amplifiers used? They are most often used in applications where low level differential signals riding on high common-mode voltages (±10V) must be extracted and accurately amplified. These applications require high input impedance, high CMRR, low input noise, low offset voltage drift and excellent gain linearity and stability.

VERY HIGH ACCURACY

A "breakthrough" in instrumentation amplifiers, the INA101 provides superior performance previously associated with expensive hybrids but now achieved at the low cost of a monolithic. A true three-op amp design allows gains of 1 to 1000V/V. The INA104 includes a fourth op-amp for increased versatility - additional gain, guard driver or offset. All circuits, including the thin-film resistors, are integrated on a single monolithic chip. The input stage uses Burr-Brown's ultra-low drift, low noise technology to provide exceptional input characteristics.

DIFFERENCE AMPLIFIER

Unity-Gain (3627): These amplifiers appear to be simple in design and assembly, but the requirement for matched components and precision adjustments makes the "build" rather than buy decision questionable. Because of our thin-film resistor technology and laser-trim skills these amplifiers offer a very cost effective solution to a common circuitry design problem.

PROGRAMMABLE GAIN AMPLIFIERS

Differential Input: 3606 is a true three-op amp instrumentation amplifier whose gain is controlled with a 4-bit digital word. Eleven differential gain steps of 1, 2, 4, 8, 16...1024V/V offer software gain control for applications where instrumentation amplifiers must operate with wide dynamic range signals while maintaining high system resolution.

Noninverting Amplifier with Multiplexed Inputs: PGA100 is a precision, digitally-programmable-gain multiplexed-input amplifier. The user can select any one of eight analog input channels simultaneously with any one of eight noninverting binarily weighted gain steps of 1, 2, 4, 8...128V/V. The digital gain and channel select are latchable for micro-processor compatible interface.

INSTRUMENTATION AMPLIFIERS

Description	Model	Range	Gain Accuracy G = 100, 25°C max	Gain Drift G = 100 ppm/°C	Non-Linearity G = 100 max	Input Parameters: CMR, DC to 60Hz, G = 10 1kΩ, Unbal...min	Input Parameters: Voltage vs Temp max (μV/°C)	Dynamic Response G = 100 ±3dB BW	Temp Range[1]	Package			Page
Very-High Accuracy	**INA104HP**	**1-1000[2]**	**0.149**	**22**	**±0.007**	**96dB**	**±50 ±400/G**	**25kHz**	**Com**	**DIP**			**27**
	INA104JP	**1-1000[2]**	**0.149**	**22**	**±0.003**	**96dB**	**±25 ±200/G**	**25kHz**	**Com**	**DIP**			**27**
	INA104KP	**1-1000[2]**	**0.149**	**22**	**±0.003**	**96dB**	**±25 ±200/G**	**25kHz**	**Com**	**DIP**			**27**
	INA101AM	1-1000[2]	0.03	22[3]	±0.007%	96dB	±(2 + 20/G)	25kHz	Ind	TO-100			2-7
	INA101CM	1-1000[2]	0.03	22[3]	±0.004%	96dB	±(0.25 + 10/G)	25kHz	Ind	TO-100			2-7
	INA101SM	1-1000[2]	0.03	22[3]	±0.004%	96dB	±(0.25 + 10/G)	25kHz	MIL	TO-100			2-7
	3630AM	1-1000[2]	0.1	125[3]	±0.007%	96dB	±(2 + 20/G)	25kHz	Ind	DIP			2-56
	3630BM	1-1000[2]	0.05	125[3]	±0.003%	96dB	±(0.75 + 10/G)	25kHz	Ind	DIP			2-56
	3630CM	1-1000[2]	0.05	125[3]	±0.003%	96dB	±(0.25 + 10/G)	25kHz	Ind	DIP			2-56
	3630SM	1-1000[2]	0.05	125	±0.003%	96dB	±(0.75 + 10/G)	25kHz	Ind	DIP			2-56
General Purpose	3626AP	5-1000[2]	0.5	35[3]	±0.05%	74dB	±(6 + 10/G)	14kHz	Ind	DIP			2-42
	3626BP	5-1000[2]	0.5	35[3]	±0.04%	80dB	±(3 + 5/G)	14kHz	Ind	DIP			2-42
	3626CP	5-1000[2]	0.5	35[3]	±0.04%	80dB	±(1 + 5/G)	14kHz	Ind	DIP			2-42
	3629AM	5-1000[2]	0.1	45[3]	±0.007%	106dB[4]	±(3 + 10/G)	30kHz	Ind	DIP			2-50
	3629AP	5-1000[2]	0.1	45[3]	±0.007%	106dB[4]	±(3 + 10/G)	30kHz	Ind	DIP			2-50
	3629BM	5-1000[2]	0.1	45[3]	±0.004%	106dB[4]	±(1.5 + 7.5/G)	30kHz	Ind	DIP			2-50
	3629BP	5-1000[2]	0.1	45[3]	±0.004%	106dB[4]	±(1.5 + 7.5/G)	30kHz	Ind	DIP			2-50
	3629CM	5-1000[2]	0.1	45[3]	±0.004%	106dB[4]	±(0.75 + 5/G)	30kHz	Ind	DIP			2-50
	3629CP	5-1000[2]	0.1	45[3]	±0.004%	106dB[4]	±(0.75 + 5/G)	30kHz	Ind	DIP			2-50
	3629SM	5-1000[2]	0.1	45[3]	±0.004%	106dB[4]	±(1.5 + 7.5/G)	30kHz	Ind	DIP			2-50
Buffer, Unity-Gain Differential	3627AM	1V/V, fixed	0.01	5	±0.001%[5]	90dB	30	800kHz[5]	Ind	TO-99			2-46
	3627BM	1V/V, fixed	0.01	5	±0.001%[5]	100dB	20	800kHz[5]	Ind	TO-99			2-46

PROGRAMMABLE GAIN AMPLIFIERS

Noninverting Multiplexed Input	PGA100AG	Gain set with 4-bit word 1, 2, 4, 8,...128	0.05	10	±0.01	NA	6[6]	5MHz	Ind	DIP			2-15
	PGA100BG		0.02	10	±0.005	NA	6[6]	5MHz	Ind	DIP			2-15
Differential Input	3606AG	Gain Set with 4-bit word 1, 2, 4 8...1024	0.05	10	0.004%	90dB, G = 1	±(3 + 50/G)	40kHz	Ind	DIP			2-34
	3606AM		0.05	10	0.004%	90dB, G = 1	±(3 + 50/G)	40kHz	Ind	DIP			2-34
	3606BG		0.02	10	0.004%	90dB, G = 1	±(1 + 20/G)	40kHz	Ind	DIP			2-34
	3606BM		0.02	10	0.004%	90dB, G = 1	±(1 + 20/G)	40kHz	Ind	DIP			2-34

PRECISION TWO-WIRE TRANSMITTER

Model	Span: Untrimmed error max	Span: Non-linearity max	Span: Temp Drift ppm%/°C	Input Parameters: Offset Voltage max	Input Parameters: Offset Voltage vs Temp max μV/°C	Input Parameters: CMR DC, min	Output Parameters: Current Range mA	Output Parameters: Offset Current error μA, max	Output Parameters: FS Output Current error μA, max	Temp Range[1]	Package			Page
XTR100AM	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	MIL/Ind	DIP			2-23
XTR100AP	−3%	0.01%	±100	±50μV	±1	90dB	4-20	±4	±20	MIL/Ind	DIP			2-23
XTR100BM	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	MIL/Ind	DIP			2-23
XTR100BP	−3%	0.01%	±100	±25μV	±0.5	90dB	4-20	±4	±20	MIL/Ind	DIP			2-23

NOTES: 1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 2) Set with external resistor. 3) With zero TC external resistor. 4) DC only. 5) Unity-gain. 6) Typical.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

ISOLATION PRODUCTS

Another facet of design, assembly and testing expertise is involved in developing and manufacturing our isolation products: amplifiers and power supplies.

Isolation amplifiers provide a signal path from the amplifier input to its output with no galvanic connection. Two techniques are used to cross the isolation barrier: transformer coupling and optical coupling.

Isolation amplifiers are useful in several ways: 1) to amplify low level signals in the presence of high common-mode voltages; 2) reduce noise by breaking ground loops; 3) protect sensitive instruments from damage by large common-mode input voltages; 4) protect patients from ground faults in patient monitoring equipment.

Our optically coupled amplifiers use a unique bifurcated optical design to greatly improve linearity and make the gain insensitive to the level of output of the LED light source used. The technique splits the LED light output - part is sent to the output amplifier (across the isolation barrier) and part is sent back to the input. This provides a stable closed loop negative feedback design and makes the gain independent of the LED output level.

ISO100 is a second generation, optically coupled ISO amp which uses a new monolithic FC designed especially for optically coupled isolation amplifiers.

The 3650 uses a differential current input stage. The 3652 uses FET inputs to provide high input impedance and allow the direct application of voltage sources.

Transformer coupled designs offer a wide range of input characteristics - uncommitted op amps of either low drift or FET input types and true three-wire instrumentation amplifier configurations. Some models provide isolated power at the input from self-contained DC-to-DC converters.

The most unique model, 3656, provides true three-port isolation (independent isolation of input, output and power supply) and provides both signal and power isolation with only one transformer.

DC-to-DC converters provide high voltage isolation from input to output and are available with dual voltage outputs of one, two or four channels per unit.

We 100% test the isolation barrier on all isolation products using a very conservative relationship of test voltage equal to two times continuous rated voltage plus 1000V.

TRANSFORMER COUPLED AMPLIFIERS

Description	Model	Isolation Voltage: Continuous (V)peak	Isolation Voltage: Pulse/Test (V)peak	Isolation Mode Rejection, min.: DC (dB)	Isolation Mode Rejection, min.: 60Hz (dB)	Leakage Current at Test Voltage (μA)	Isolation Impedance: Ω	Isolation Impedance: pF	Gain Nonlinearity: max. (%)	Gain Nonlinearity: typ. (%)	Voltage Drift ±μV/°C max	Bias Current max	±3dB Freq. kHz	External Isolation Power Required	Temp. Range[1]	Package			Page
Low Drift[2]	3450	±500	±2000	160	120	1	10^{12}	16	±0.005	±0.0015	100	50nA	1.5	No	Com	Module			3-19
Low Bias FET	3451	±500	±2000	160	120	1	10^{12}	16	±0.025	±0.005	100	25pA	2.5	No	Com	Module			3-19
	3452	±2000	±5000	160	120	1	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module			3-19
	3455	(3)	(3)	160	120	(3)	10^{12}	16	±0.025	±0.005	100	20pA	2.5	No[4]	Com	Module			3-19
True 3-wire Inst. Amp	3456A	±2000	±5000	160	130	25	10^{12}	14	±0.02	±0.01	2 + (150/G)	50nA	2.5	No	Com	Module			3-26
	3456B	±2000	±5000	160	130	25	10^{12}	14	±0.08	±0.03	1 + (75/G)	50nA	2.5	No	Com	Module			3-26
Highest Isolation Voltage	3656AG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	25 + (500/G)	100nA	30	No	Ind	DIP			3-40
	3656BG	±3500	±8000	160	125	0.5	10^{12}	6	±0.05	±0.03	5 + (350/G)	100nA	30	No	Ind	DIP			3-40
	3656HG	±3500	±8000	160	125	0.5	10^{12}	6	±0.15	±0.03	200 + (1000/G)	100nA	30	No	Com	DIP			3-40
	3656JG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	50 + (750/G)	100nA	30	No	Com	DIP			3-40
	3656KG	±3500	±8000	160	125	0.5	10^{12}	6	±0.1	±0.03	10 + (350/G)	100nA	30	No	Com	DIP			3-40

OPTICALLY COUPLED AMPLIFIERS

Description	Model	Isolation Voltage: Continuous (V)peak	Isolation Voltage: Pulse/Test (V)peak	Isolation Mode Rejection, min.: DC (dB)	Isolation Mode Rejection, min.: 60Hz dB	Leakage Current at Test Voltage (μA)	Isolation Impedance: Ω	Isolation Impedance: pF	Gain Nonlinearity: max. (%)	Gain Nonlinearity: typ. (%)	Voltage Drift ±μV/°C max	Bias Current max	±3dB Freq. kHz	External Isolation Power Required	Temp. Range[1]	Package			Page
Balanced Current Input	3650HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	25	10nA	15	Yes[6]	Ind	DIP			3-32
	3650JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.03	10	10nA	15	Yes[6]	Ind	DIP			3-32
	3650KG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.05	±0.02	5	10nA	15	Yes[6]	Ind	DIP			3-32
	3650MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	10nA	15	Yes[6]	Ind	DIP			3-32
Balanced FET Input	3652HG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	50	50nA	15	Yes[6]	Ind	DIP			3-32
	3652JG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.1	±0.05	25	50nA	15	Yes[6]	Ind	DIP			3-32
	3652MG	±2000	±5000	140	120	0.25[5]	10^{12}	1.8	±0.2	±0.05	100	50nA	15	Yes[6]	Ind	DIP			3-32
Low Drift Wide Bandwidth	ISO100AP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.4	0.1	10^{7}	10nA	60	Yes[6]	Ind	DIP			3-6
	ISO100BP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.1	0.03	4^{7}	10nA	60	Yes[6]	Ind	DIP			3-6
	ISO100CP	750	2500	146[7]	108[7]	0.3	10^{12}	2.5	0.07	0.02	4^{7}	10nA	60	Yes[6]	Ind	DIP			3-6

DC/DC CONVERTERS

Description	Model	Input	Output	Isolation	Leakage Current	Package			Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module			8-3
Isolated	722/722BG	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA/160mA	3500V[8] 8000V[9]	1μA at 240V, 60Hz	DIP			8-13
	724	5VDC to 16VDC 125mA	Four-Bipolar +8V	1000V[8] 3000V[9]	1μA at 240V, 60Hz	DIP			8-17

NOTES: 1) Com =0°C to +70°C; Ind = −25°C to +85°C. 2) Bipolar. 3) Isolation voltage tested at 2500V, rms, 60Hz; leakage current tested for 2μA max at 240V, rms, 60Hz. 4) ±15V at ±15mA isolated power available to power external circuitry. 5) At 240V/60Hz. 6) Models 722 or 724. 7) R_{IN} = 10k, Gain = 100. 8) Continuous. 9) Test.

FIBER OPTIC DATA LINKS

Total noise immunity and electrical isolation are provided by these fiber optic data links designed to convert TTL or analog input signals to output light signals and transmit data - with maximum accuracy - through severe electrical environments.

This FOT/FOR110 DC-coupled link is data pattern independent. Special coding is not required and asynchronous data can be accepted.

FOT114 is a self-contained transmitter whose output is a train of light pulses whose frequency is directly proportional to the magnitude of an analog input signal. It's capable of transmitting analog signals as small as 10mV FS up to 9.0km with a linearity error of ±0.005%.

FOT110 transmitter/FOR110 receiver are compact IC packages 2.1" x 1.1" x 0.4" (43.1mm x 27.9mm x 10.1mm) that transmit TTL inputs at data rates of 0 to 2M bits at distances up to 6.0km without repeaters. They also can transmit analog signals as amplitude modulation of the light output in a 10Hz to 1MHz bandwidth.

SPECIAL OFFER* — COMPLETE DATA LINK — SAVE 45%

Here is an easy and inexpensive way to evaluate fiber optics in your application. Each FODL (Fiber Optic Data Link) contains a transmitter, receiver, two electrical sockets and factory terminated fiber optic cable. Apply power and you have a complete functioning link ready for experimentation in your own application. FODL-K4-IR, $147.50; FODL-K6, $188; FODL-K6-IR, $192.

*Limit one of each link per customer.

FIBER OPTICS

Transmitter/Receiver	Input	Output	Data Rate	Wavelength	Link Length[1]	Auto-Threshold™	Adjustable Light Output	Price ($)[2]		FODL[3] Number	Page
FOT110KG/FOR110KG	TTL	TTL	0 to 2M bits	665nm	1900M[4]	Yes	Yes			FODL-K4	4-2
FOR110KG-IR/FOR110KG	TTL	TTL	0 to 1M bits	880nm	6000M[5]	Yes	Yes			FODL-K4-IR	4-2
FOT114KG/FOR110KG	**Analog**	**TTL**	**0-100kHz**	**665nm**	**2400M**	**Yes**	**Yes**			**FODL-K5**	**38**
FOT114KG-IR/FOR110KG	**Analog**	**TTL**	**0-100kHz**	**880nm**	**9700M**	**Yes**	**Yes**			**FODL-K6**	**38**
3712T/3712R	TTL	TTL	0 to 25k bits	670nm	2290M[6]	Yes	No			FODL-K1	4-14
3713T/3713R	TTL	TTL	0 to 250k bits	660nm	2500M[6]	Yes	Yes			FODL-K2	4-22
3714T/3713R	Analog	TTL[7]	0 to 10kHz	660nm	2500M[6]	Yes	Yes			FODL-K3	4-30

FIBER OPTIC CABLE ASSEMBLIES							
Model	Conditions	Core Material	Attenuation	Numerical Aperature	Rise Time		Page
OCA100	$\lambda = 660$nm	Plastic	1300dBm/km	0.53	—		4-10
OCA101	$\lambda = 660$nm	Plastic	360dBm/km	0.53	5.5nsec/km		4-10
OCA102	$\lambda = 660$nm	Silica	33dBm/km	0.40	3.8nsec/km		4-10
OCA201	**$\lambda = 665$nm**	**Plastic**	**0.25dB/m**	**0.50**	-		**50**

NOTES: 1) Without repeaters. 2) Transmitter and receiver may be purchased separately. 3) See "Special Offer" above. 4) 200μm core dia., 12dB/km attenuation. 5) 63μm core dia., 2dB/km attenuation. 6) 200μm core dia., 8dB/km attenuation. 7) May be converted to analog with a Voltage-to-Frequency converter.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

Q PROGRAM

MIL-STD-883 RELIABILITY SCREENING

Burr-Brown's Q Program offers increased reliability of standard Burr-Brown integrated circuits at reasonable cost. The Q Program is applicable to military and aerospace programs, as well as in industrial process control, medical patient monitoring and other applications where product failure may be expensive or hazardous. The Q Program consists of screening standard Burr-Brown integrated circuit products in accordance with applicable test methods of MIL-STD-883. The screening sequence below details the mechanical, electrical, and thermal stresses applied to 100% of the Q products to identify and remove any potentially failure-prone devices. Burr-Brown brochure LI-217 describes the Q products testing procedure in detail.

Burr-Brown products available with "Q" screening include converters, op amps, multipliers, sample/holds, and filters. "Q" products are identified in this selection guide by "Q" following the model number.

SCREENING SEQUENCE

Screen	Procedure*	Requirement/ Performed
Internal Visual Inspection (precap)	Burr-Brown QC4118 (copies available on request)	100%
Electrical Test	Per appropriate Burr-Brown product data sheet	100%
Stabilization Bake	MIL-STD-883, Method 1008	100%
Temperature Cycling	MIL-STD-883, Method 1010	100%
Hermeticity, Fine Leak	MIL-STD-883, Method 1014	100%
Hermeticity, Gross Leak	MIL-STD-883, Method 1014	100%
Burn-In	MIL-STD-883, Method 1015	100%
Constant Acceleration (centrifuge)	MIL-STD-883, Method 2001	100%
Final Electrical Test	Per appropriate Burr-Brown product data sheet	100%
External Visual Inspection	Burr-Brown QC5150 (copies available on request)	100%

*See detailed Screening Procedures for each product.

ANALOG CIRCUIT FUNCTIONS

These circuits offer a broad range of versatile, proven and ready-to-use analog computational functions designed to work in simple and complex instrumentation and control systems. Primarily they process and/or condition analog signals - usually for simulation of algebraic or trigonometric computations. Burr-Brown has the widest selection of such functions available in the industry. How you apply these circuits is limited only by your creative imagination!

MULTIPLIERS/DIVIDERS

You can select accuracy from 0.25% to 2% max from this complete line of integrated circuit multipliers. Most provide full four-quadrant multiplication. All are laser-trimmed for accuracy - no trim pots are needed to meet specified performance. These compact models bring the cost of high performance down to acceptable levels.

MULTIPLIERS/DIVIDERS											
Model[1]	Transfer Function	Error max at 25°C %, max	Temperature Coefficient %/°C	Feed-through mV	Offset Voltage mV	1% Bandwidth kHz	Temp Range[2]	Package			Page
4203J	$XY/10$	2	0.04	50	20	40	Com	TO-100			5-41
4203K	"	1	0.04	50	20	40	Com	TO-100			5-41
4203S, (Q)	"	1	0.04	50	20	40	MIL	TO-100			5-41
4204J	"	0.5	0.01	10	15	32	Ind	DIP			5-43
4204K	"	0.5	0.01	5	5	33	Ind	DIP			5-43
4204S, (Q)	"	0.25	0.02	5	5	33	MIL	DIP			5-43
4205J	$(X_1 - X_2)(Y_1 - Y_2)/10$	2	0.04	50	20	40	Com	TO-100			5-41
4205K	"	1	0.04	50	20	40	Com	TO-100			5-41
4205S, (Q)	"	1	0.04	50	20	40	MIL	TO-100			5-41
4206J	$XY/10$	0.5	0.01	10	15	33	Com	DIP			5-49
4206K	"	0.25	0.01	5	5	33	Com	DIP			5-49
4213AM, (Q)	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.008	30	10	70	Ind	TO-100			5-55
4213BM	"	0.5	0.008	30	7	70	Ind	TO-100			5-55
4213SM	"	0.5	0.008	30	7	70	MIL	TO-100			5-55
4213/MIL Series		See Military Products, Page xvii									
MPY100A	**$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z_2$**	**±2**	**0.017**	**100**	**50**	**70**	**Ind**	**TO-100**			**52**
MPY100B	"	**±1**	**0.008**	**30**	**10**	**70**	**Ind**	**TO-100**			**52**
MPY100C	"	**±0.5**	**0.008**	**30**	**7**	**70**	**Ind**	**TO-100**			**52**
MPY100S	"	**±0.5**	**0.025**	**30**	**7**	**70**	**MIL**	**TO-100**			**52**
4214AP	$[(X_1 - X_2)(Y_1 - Y_2)/10] + Z$	1	0.02	30	10	70	Ind	DIP			5-62
4214BP	"	0.5	0.02	30	7	70	Ind	DIP			5-62
4214RM	"	1	0.02	30	10	70	Ind	DIP			5-62
4214SM	"	0.5	0.02	30	7	70	Ind	DIP			5-62

*Same as model above. NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x.
2) Com = 0°C to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

DIVIDERS

The use of a special log/antilog committed divider design overcomes the major problem encountered when trying to use a multiplier in a divider circuit. Outstanding accuracy is maintained even at very low denominator voltages.

DIVIDERS											
Model	Transfer Function	Input Range	Accuracy, max D = 250mV %	Temperature Coefficient %/°C	0.5% Bandwidth kHz	Rated Output, min	Temp Range[1]	Package			Page
DIV100HP	N/D 10	250mV	1.0	0.2	15	±10V, ±5mA	Ind	DIP			5-6
DIV100JP	*	to	0.5	0.2	15	±10V, ±5mA	Ind	DIP			5-6
DIV100KP	*	10V	0.25	0.2	15	±10V, ±5mA	Ind	DIP			5-6

*Same as model above NOTES: 1) Ind = −25°C to +85°C.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

SPECIAL FUNCTIONS

This group of models offers many different functions that are the quick, easy way to solve a wide variety of analog computational problems. Most are in integrated circuit packages and are laser-trimmed for excellent accuracy.

Function	Model	Description	Comments	Temp Range[1]	Package			Page
Multifunction Converter	4301 4302	$Y(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	4301 is hermetically sealed and shielded in a metal package. 4302 is in a plastic package. Both units are pin-for-pin compatible.	Ind Ind	DIP DIP			5-66 5-68
	LOG100JP	$X(Z/X)^m$ This function may be used to multiply, divide, raise to powers, take roots and form sine and cosine functions.	Optimized for log ratio of current inputs. Specified over six decades of input (1nA to 1mA), 55mV total error, 0.25% log conformity.	Com	DIP			5-14
Logarithmic Amplifier	4127JG 4127KP	K Log (I_1/I_{REF})	A more versatile part which contains an internal reference and a current inverter. 1% and 0.5% accuracy.	Com Com	DIP DIP			5-34 5-34
$\sqrt{\frac{1}{T}\int_0^T E_{IN}^2 \cdot dt}$	4340	True rms-to-DC conversion based on a log-antilog computational approach.	Laser-trimmed, requires no external trimming for rated accuracy. Hermetically sealed in a metal package.	Ind	DIP			5-74
	4341	True rms-to-DC conversion based on a log-antilog computational approach.	Some external trimming required. Lower cost in plastic package. Pin compatible with 4340.	Ind	DIP			5-78
Peak Detector	4085BM 4085KG 4085SM	These are analog memory circuits which hold and provide read-out of a DC voltage equal to peak value of a complex input waveform.	Digital mode control provides reset capability and allows selection of peaks within a desired time interval. May be used to make peak-to-peak detector.	Com Ind MIL	DIP DIP DIP			5-26 5-26 5-26
Window Comparator	4115/04	4115/04 provides a window or dual limit for comparison. Unit has 3 inputs: one for a voltage that sets upper limit, one for a voltage that sets lower limit, and one for a signal input.	The 3 outputs are capable of sinking up to 200mA of current, indicating if the input voltage is above, below, or in the window.	Com	Module			5-32
Level Comparator	4082/03	Compares input voltage with user set limit. Provides 2-state logic output that indicates whether one analog voltage is > or < another.	Adjustable hysteresis uncommitted collector output can sink up to 100mA.	Ind	DIP			5-24

NOTE: 1) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

FREQUENCY PRODUCTS

This group of products consists of precision oscillators and active filters for both signal generation and attentuation. Both fixed frequency and user selected frequency units are available.

Function	Model	Description	Comments	Temp Range[1]	Package			Page
Oscillator	4023/25	Fixed-frequency (customer-specified, 10Hz to 20kHz) provides a low distortion, stable amplitude sine wave output.	Frequency stability vs temperature: 0.04%/°C max. Amplitude stability vs temperature: 0.02%/°C max.	Ind	Module			5-22
	4423	Very-low cost in plastic package. Provides resistor programmable quadrature outputs (sine and cosine wave outputs simultaneously available.)	Frequency range: 0.002Hz to 20kHz. Frequency stability: 0.01%/°C. Quadrature phase error: ±0.1%.	Com	DIP			5-82
Universal Active Filter	UAF41 UAF31 UAF21 UAF21H UAF11 UAF11H	These filters provide a complex pole pair. Based on state variable approach, low-pass, high-pass and bandpass outputs are available.	Add only resistors to determine pole location (frequency and Q). Easily cascaded for complex filter responses.	Ind Ind Ind Ind Ind Ind	DIP DIP DIP DIP DIP DIP			5-109 5-101 5-93 5-93 5-93 5-93

Function	Model	Description	Comments	Temp Range[1]	Package			Page
Fixed-Frequency Active Filter	ATF76 Series	Over 60 different types of filters are available from combinations of filter type, number of poles and type of response.	Low-pass, bandpass and band reject. Butterworth, Chebyschev and Bessel. 2 to 8 poles.	Ind	DIP			5-86

NOTE: 1) Com = 0 to +70°C; Ind = −25°C to +85°C.

VOLTAGE REFERENCE

This product is a precision voltage reference which provides a +10V output. The output can be adjusted with minimal effect on drift or stability.

Model	Output (V)	Minimum Output (mA)	Maximum Drift (ppm/°C)	Power Supply (V)	Power Supply (mA)	Temp Range[1]	Package			Page
REF101KM	**+10,000 ±0.005**	**10**	**1**	**+13.5/35**	**4.5**	**Com**	**TO-99**			**60**
REF101JM	**+10,000 ±0.005**	**10**	**2**	**+13.5/35**	**4.5**	**Com**	**TO-99**			**60**
REF101SM	**+10,000 ±0.005**	**10**	**3**	**+13.5/35**	**4.5**	**MIL**	**TO-99**			**60**
REF101RM	**+10,000 ±0.005**	**10**	**6**	**+13.5/35**	**4.5**	**MIL**	**TO-99**			**60**

NOTES: 1) Com = 0 to +70°C; MIL = −55°C to +125°C.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

DATA CONVERSION DATA ACQUISITION

Designing, assembling and testing high performance data converters and data acquisition systems - including models that have become industry standards - allows us to offer you complete, practical, easily applied solutions to difficult problems.

We have established a full line of interrelated digital and analog products whose functions are complementary and thereby give you one-stop shopping - Burr-Brown! We simplify your design task by applying powerful analog and digital expertise - employing high level integration to create complete products that don't require extensive external components. Our application of microcomputer technology and compatibility makes it much easier for you to interface our products. Even engineers with limited analog experience design-in these versatile circuits with confidence.

ANALOG-TO-DIGITAL CONVERTERS

These designs will meet your most demanding applications. We employ monolithic technology to support the high performance offered. The successive-approximation design approach produces ADC's that give 12-bit conversion in as low as 1.5μsec, 8-bit conversion in less than 3μsec, and low cost 12-bit designs that convert in 25μsec. High resolution 16-bit converters in small DIL packages give conversions to 0.003% accuracy in 15μsec at a very reasonable price. Harsh temperature environments can be handled as well with 12-bit converters that operate to +200°C.

ANALOG-TO-DIGITAL CONVERTERS

Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Conversion Time, max (μsec)	Accy Drift Bipolar, max (ppm FSR/°C)	Input Range (V)	Temp Range[2]	Package			Page
Low Cost	ADC80AG-10[3]	10	±0.048	21	±23	±2.5, ±5,	Ind	Ceramic			6-48
	ADC80AG-12[3]	12	±0.012	25	±23	±10, +5, +10	Ind	32-pin DIP			6-48
Low Cost, High Speed	ADC82AG	8	±0.2	2.8	±60	±2.5, ±5, ±10	Ind	24-pin DIP			6-56
	ADC82AM, (Q)	8	±0.2	2.8	±60	+5, +10, +20	Ind				6-56
	ADC84KG-10	10	±0.048	6	±21	±2.5, ±5, ±10	Com	32-pin DIP			6-64
	ADC84KG-12	12	±0.012	10	±21	+5, +10	Com				6-64
Low Drift, High Speed	AD85C-10	10	±0.048	6	±26	±2.5, ±5	Com	Metal Hermetic 32-pin DIP			6-64
	ADC85-10	10	±0.048	6	±16	±10, +5, +10	Ind				6-64
	ADC85C-12, (Q)	12	±0.012	10	±19		Com				6-64
	ADC85-12, (Q)	12	±0.012	10	±13		Ind				6-64
Very High Speed	**ADC803BM**	**12**	**±0.020**	**1.5**	**±23**	**±5, ±10, 0 to −10**	**Ind**	**Metal Hermetic 32-pin DIP**			**79**
	ADC803CM	**12**	**±0.015**	**1.5**	**±23**		**Ind**				**79**
High Resolution, High Accuracy	**ADC73J**	**16**	**±0.0015**	**170**	**±9**	**±5, ±10, 0 to +10 0 to +20**	**Com**	**Module**			**68**
	ADC73K	**16**	**±0.00075**	**170**	**±9**		**Com**	**Module**			**68**
	ADC731J	**16**	**±0.0015**	**170**	**±9**		**Com**	**Module**			**68**
	ADC731K	**16**	**±0.00075**	**170**	**±9**		**Com**	**Module**			**68**
High Resolution	ADC71JG	16	±0.006	50	±15	±2.5, ±5, ±10, 0 to +5, 0 to +10, 0 to +20	Com	Ceramic 32-pin DIP			6-24
	ADC71KG	16	±0.003	50	±15		Com				6-24
	ADC72AM	16	±0.006	50	±12		Ind	Metal Hermetic 32-pin DIP			6-32
	ADC72BM	16	±0.003	50	±12		Ind				6-32
	ADC72JM	16	±0.006	50	±17		Com				6-32
	ADC72KM	16	±0.003	50	±17		Com				6-32
	ADC76JG	16	±0.006	15	±15		Com	Ceramic 32-pin DIP			6-40
	ADC76KG	16	±0.003	15	±15		Com				6-40

ANALOG-TO-DIGITAL CONVERTERS											
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Conversion Time, max (μsec)	Accy Drift Bipolar, max (ppm FSR/°C)	Input Range (V)	Temp Range[2]	Package			Page
Very-Wide Temp Range	ADC10HT ADC10HT-1	12 12	±0.012 ±0.048	50 50	±34 ±63	±5, ±10 ±5, ±10	−55°C to +200°C	Ceramic 28-pin DIP			6-8 6-8
High Speed	ADC60-08 ADC60-10 ADC60-12	8 10 12	±0.195 ±0.0488 ±0.0244	0.88 1.88 3.50	±20 ±20 ±15	±2.5, ±5 ±10, +5 +10, +20	Com Com Com	Module Module Module			6-18 6-18 6-18
Military	ADC87/MIL Series	See Military Products, page xvii									
High Resolution	ADC100-SMD	4 digit + sign	±0.005	30msec	±5	±10	Com	Module			6-72
PCM Audio Converter	PCM75	See Special Products, page xvii									

NOTES: 1) "Q" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C. 3) "Z" models operate from ±12VDC supply.

DIGITAL-TO-ANALOG CONVERTERS

Our DAC80 is a standard in 12-bit performance. DAC800 - a monolithic IC - continues this proven product offering the same pinout, functions and improved performance at a lower price.

16-bit designs from Burr-Brown have also set industry standards: DAC71 is the industry standard low-cost 16-bit D/A; DAC701 and DAC703 are complete 16-bit monolithics with op amps and voltage reference on the chip.

ECL-compatible DAC63 employs new technology and higher levels of integration to achieve 35nsec (typ to ±0.012%) settling time and excellent temperature and time stability at low cost.

DIGITAL-TO-ANALOG CONVERTERS											
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Accy Drift Bipolar, max (ppm FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Temp Range[2]	Package			Page
High Resolution Monolithic	**DAC701KH** **DAC701BH** **DAC703KH** **DAC703BH**	**16** **16** **16** **16**	**±0.003** **±0.003** **±0.003** **±0.003**	**±28** **±28** **±25** **±25**	**0 to +10V** **0 to +10V** **±10V** **±10V**	**4μsec** **4μsec** **4μsec** **4μsec**	**Com** **Ind** **Com** **Ind**	**Ceramic Hermetic 24-pin DIP**			**91** **91** **91** **91**
Monolithic[3] 12-Bit	DAC800-CBI-I DAC800-CBI-V DAC800P-CBI-V	12 12 12	±0.012 ±0.012 ±0.012	±25[3] ±25 ±25	±1, −2mA ±2.5, ±5, ±10V +5, +10V	300nsec 3μsec 3μsec	Com Com Com	Ceramic 24-pin DIP Plastic 24-pin DIP			6-183 6-183
	DAC850-CBI-I DAC850-CBI-V	12 12	±0.012 ±0.012	±17[3] ±17	±1, −2mA ±2.5, ±5, ±10, +5, +10V	300nsec 3μsec	Ind Ind	Ceramic Hermetic 24-pin DIP			6-190 6-190
	DAC851-CBI-I DAC851-CBI-V	12 12	±0.012 ±0.012	±30[3] ±30	±1, −2mA, ±2.5, ±5, ±10, +5, +10V	300nsec 3μsec	MIL MIL	Ceramic Hermetic 24-pin DIP			6-190 6-190
Low Cost	DAC80-CBI-I[4] DAC80-CBI-V[4] DAC80-CCD-I[4] DAC80-CCD-V[4]	12 12 3 digits 3 digits	±0.012 ±0.012 ±0.025 ±0.025	±25[5] ±25 ±25[5] ±25	±1.0, −2mA ±2.5, ±5, ±10 +5, +10V 0 to −2mA 0 to +10V	300nsec 3μsec 300nsec 3μsec	Com Com Com Com	Ceramic 24-pin DIP			6-152 6-152 6-152 6-152
Low Drift	DAC85-CBI-I, (Q) DAC85-CBI-V, (Q) DAC85C-CBI-I, (Q) DAC85C-CBI-V, (Q) DAC85LD-CBI-V	12 12 12 12 12	±0.012 ±0.012 ±0.012 ±0.012 ±0.012	±20[5] ±20 ±30[5] ±30 ±5	±1.0, −2mA ±2.5, ±5, ±10 +5, +10V ±1.0, −2mA ±2.5, ±5, ±10 +5, +10V ±2.5, ±5, ±10 +5, +10V	300nsec 3μsec 300nsec 3μsec 3μsec	Ind Ind Com Com Ind	Metal Hermetic 24-pin DIP			6-170 6-170 6-170 6-170 6-170
High Resolution	DAC70-CSB-I DAC70-COB-I, (Q) DAC70C-CSB-I DAC70C-COB-I DAC70-CCD-I DAC70C-CCD-I	16 16 16 16 4 digits 4 digits	±0.003 ±0.003 ±0.005 ±0.005 ±0.003 ±0.005	±7[5] ±7[5] ±10[5] ±10[5] ±7[5] ±10[5]	0 to −2mA ±1mA 0 to −2mA ±1mA 0 to −2mA 0 to −2mA	50μsec 50μsec 50μsec 50μsec 50μsec 50μsec	Ind Ind Com Com Ind Com	Metal Hermetic 24-pin DIP			6-101 6-101 6-101 6-101 6-101 6-101

DIGITAL-TO-ANALOG CONVERTERS											
Description	Model[1]	Resolution (Bits)	Linearity Error max (% of FSR)	Accy Drift Bipolar, max (ppm FSR/°C)	Output Ranges	Settling Time (FSR, ±1/2LSB)	Temp Range[2]	Package			Page
High Resolution	DAC71-CSB-I	16	±0.003	±15[5]	0 to −2mA	1μsec	Com	Ceramic 24-pin DIP			6-109
	DAC71-COB-I	16	±0.003	±15[5]	±1mA	1μsec	Com				6-109
	DAC71-CCD-I	4 digits	±0.005	±15[5]	0 to −2mA	1μsec	Com				6-109
	DAC71-CSB-V	16	±0.003	±15	0 to +10V	10μsec	Com				6-109
	DAC71-COB-V	16	±0.003	±15	±10V	10μsec	Com				6-109
	DAC71-CCD-V	4 digits	±0.005	±15	0 to +10V	10μsec	Com				6-109
	DAC72C-CSB-I	16	±0.003	±15[5]	0 to −2mA	1μsec	Com	Metal Hermetic 24-pin DIP			6-119
	DAC72C-COB-I	16	±0.003	±15[5]	±1mA	1μsec	Com				6-119
	DAC72C-CCD-I	4 digits	±0.005	±15[5]	0 to −2mA	1μsec	Com				6-119
	DAC72C-CSB-V	16	±0.003	±15	0 to +10V	10μsec	Com				6-119
	DAC72C-COB-V	16	±0.003	±15	±10V	10μsec	Com				6-119
	DAC72C-CCD-V	4 digits	±0.005	±15	0 to +10V	10μsec	Com				6-119
	DAC72-CSB-I	16	±0.003	±19[5]	0 to −2mA	1μsec	Ind	Metal Hermetic 24-pin DIP			6-119
	DAC72-COB-I	16	±0.003	±19[5]	±1mA	1μsec	Ind				6-119
	DAC72-CCD-I	4 digits	±0.005	±19[5]	0 to −2mA	1μsec	Ind				6-119
	DAC72-CSB-V	16	±0.003	±19	0 to +10V	10μsec	Ind				6-119
	DAC72-COB-V	16	±0.003	±19	±10V	10μsec	Ind				6-119
	DAC72-CCD-V	4 digits	±0.005	±19	0 to +10V	10μsec	Ind				6-119
High-Resolution Highly Accurate	DAC73J	16	±0.015	±22	±2.5, ±5, ±10 +5V, +10V 0 to −2mA	50μsec	Com	Module			6-129
	DAC73K	16	±0.00075	±22		50μsec	Com	Module			6-129
	DAC736J	16	±0.0015	±22		50μsec	Com	Module			6-129
	DAC736K	16	±0.00075	±22	±1mA	50μsec	Com	Module			6-129
Very-Wide Temperature Range	DAC10HT	12	±0.012	±20	±2.5, ±5, ±10, +5, +10	200nsec	−55°C to +200°C	Ceramic 24-pin DIP			6-80
	DAC10HT-1	12	±0.048	±50		200nsec					6-80
Very-High Speed	DAC60-10	10	±0.048	±15[5]	0 to −5mA ±2.5mA	40nsec	Com	Module			6-88
	DAC60-12	12	±0.012	±15[5]		150nsec	Com	Module			6-88
Ultra-High Speed	DAC63BG	12	±0.012	±21	±5, −10mA	35nsec	Ind	Ceramic 24-pin DIP			6-93
	DAC63CG	12	±0.012	±16	±5, −10mA	35nsec	Ind				6-93
	DAC63BM	12	±0.012	±21	±5, −10mA	35nsec	Ind	Metal Hermetic 24-pin DIP			6-93
	DAC63CM	12	±0.012	±16	±5, −10mA	35nsec	Ind				6-93
Military	DAC87/MIL Series	See Military Products, page xvii									
Low Cost	DAC82KG	8	±0.16	±50	±2.5, ±5, ±10 +5, +10V; ±0.8, 0 to −1.6mA	2.5μsec	Com	Ceramic 18 pin DIP			6-163
Monolithic 8-Bit	DAC90BG, (Q)	8	±0.2	±75[5]	±1, −2mA	200nsec	Ind	Ceramic Hermetic 16-pin DIP			6-178
	DAC90SG, (Q)	8	±0.2	±75[5]	±1, −2mA	200nsec	MIL				6-178
PCM Audio Converter	PCM50KG PCM52/53	See Special Products, Page xvii									

POWER DIGITAL-TO-ANALOG CONVERTER										
Description	Model	Input Coding	Accuracy	Tempco (ppm FSR/°C)	Output Voltage (V)	Output Current (mA)	Package			Page
Low Cost Open PC Card	4804	12-bit Binary	±0.05% of Reading	50, max	User-selected to ±30	±2000	PC Card			6-381

NOTES: 1) "Q" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C. 3) In −V models the output op amp is on a second chip. 4) "Z" models operate from ±12VDC supply. 5) When used with an external op amp which uses the internal feedback resistor.

SELF-CALIBRATING, HIGH PRECISION D/A CONVERTER

This unique 16-bit D/A converter is actually an instrument. The heart is a highly accurate 16-bit D/A converter with a heated, temperature compensated precision reference. Wrapped around this D/A are microcomputer-controlled measurement and calibration circuits that automatically null out gain, offset and linearity errors caused by shifts with time and temperature when initated by one negative-going TTL-pulse provided by the user.

SELF-CALIBRATING D/A CONVERTER								
Description	Model	Resolution	Total Error +15°C to +45°C	Output Ranges	Calibration Time	Package		Page
Precision, High-Resolution	DAC74	16 bits	±0.0015%, max	0 to +10V ±10V	2.5sec, initiated by 14μsec negative TTL pulse	7" x 5" x 0.600" metal		6-137

VOLTAGE-TO-FREQUENCY CONVERTERS

VFC's provide a simple low cost way of converting analog signals into digital form. They produce a pulse train with a repetition rate proportional to the amplitude of the analog input. The combination of accuracy, linearity, and low temperature drift make these units some of the best available. Simple low cost isolation is obtained when a VFC is used together with a DC/DC converter and a single optical coupler.

V/F CONVERTERS										
Description	Model[1]	Frequency Range (kHz)	V_{IN} Range (V)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Temp Range[2]	Package			Page
Low Drift	VFC12	0 to 10	0 to +10	±0.01	±50	Ind	Module			6-360
Complete	VFC15	0 to 20	0 to +20	±0.01	±50	Ind	Module			6-360
Very-Low Drift,	VFC12LD	0 to 10	0 to +10	±0.005	±10	Ind	Module			6-360
Complete	VFC15LD	0 to 20	0 to +20	±0.005	±10	Ind	Module			6-360
Low Cost,	VFC32KP	User-	User-	±0.01 at 10kHz	75 typ	Com	DIP			6-367
Monolithic	VFC32BM, (Q)	selected,	selected	±0.05 at 100kHz	±100	Ind	TO-100			6-367
	VFC32SM, (Q)	500kHz, max		±0.2 at 500kHz	±150	MIL	TO-100			6-367
Military	VFC32/MIL Series	See Military Products, page xvii								
Low Cost	VFC42BP	0 to 10	0 to +10	±0.01	±100	Ind	DIP			6-375
	VFC42SM	0 to 10	0 to +10	±0.01	±100	MIL	DIP			6-375
	VFC52BP	0 to 100	0 to +10	±0.05	±150	Ind	DIP			6-375
	VFC52SM	0 to 100	0 to +10	±0.05	±150	MIL	DIP			6-375
Precision	**VFC62BG**	**User-selected, 1MHz max**	**User-selected**	**±0.005 at 10kHz**	**±50**	**Ind**	**DIP**			**101**
	VFC62BM			**±0.005 at 10kHz**	**±50**	**Ind**	**TO-100**			**101**
	VFC62SM			**±0.005 at 10kHz**	**±50**	**MIL**	**TO100**			**101**
	VFC62CG			**±0.002 at 10kHz**	**±20**	**Ind**	**DIP**			**101**
	VFC62CM			**±0.002 at 10kHz**	**±20**	**Ind**	**TO-100**			**101**
	VFC320BG			**±0.005 at 10kHz**	**±50**	**Ind**	**DIP**			**109**
	VFC320BM			**±0.005 at 10kHz**	**±50**	**Ind**	**TO-100**			**109**
	VFC320SM			**±0.005 at 10kHz**	**±50**	**MIL**	**TO-100**			**109**
	VFC320CG			**±0.002 at 10kHz**	**±20**	**Ind**	**DIP**			**109**
	VFC320CM			**±0.002 at 10kHz**	**±20**	**Ind**	**TO-100**			**109**

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) Com = 0 to +70°C; Ind = −25°C to +85°C; MIL = −55°C to +125°C.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

DATA ACQUISITION SYSTEMS

Designed for high performance general purpose applications, these systems provide a complete data acquisition function in one small package. You can devote your design efforts to other tasks because the totally self-contained system includes input multiplexer, instrumentation amplifier (in some models), sample-and-hold amplifier and 12-bit A/D converter. Timing and control logic, clock and reference are all internal. A host of features - even tri-state outputs for microprocessor buses - make this system practical, even in high volume buys.

DATA ACQUISITON SYSTEMS									
Description	Model	Channels	Resolution (Bits)	Throughput Accuracy (% of FSR)	Throughput Rate (kHz)	Package			Page
Modular	SDM853	16 single-ended 8 differential	12	±0.025	30[1]	Module			6-308
Low Level	SDM858	16 single-ended 8 differential	12	±0.025[2]	8[1]	Module			6-336
Hybrid	SDM854AG	16 single-ended	12	±0.048	40	QIP[3]			6-314
±10V Input	SDM854BG	8 differential	12	±0.024	29	QIP			6-314
Hybrid	SDM856JG	**16 single-ended**	12	±0.048	33	QIP			6-330
	SDM856KG	**8 differential**	12	±0.024	25	QIP			6-330
Hybrid	SDM857JG	**16 single-ended**	12	±0.048	25	QIP			6-330
Low Level	SDM857KG	**8 differential**	12	±0.024	18	QIP			6-330

NOTES: 1) Can be increased if short-cycled to 8- or 10-bit resolution 2) At gain = 100. 3) 80-pin Quad-in-line Ceramic package, 1.7" x 2.18" x 0.23".

MICROPROCESSOR INTERFACED ANALOG INPUT AND OUTPUT SYSTEMS

These data acquisition and analog data distribution systems are complete - totally interfaced to the microprocessor bus with no external interfacing components required. They provide an instant solution by preserving your valuable engineering design resources. 16-channel analog input systems and two-channel analog output systems talk directly to popular buses under control of the microprocessor. They are truly design-in-and-forget solutions to analog interface problems.

MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS

Description	Model	Channels	Resolution	Accuracy (% of FSR) max	Tempco (ppm/°C) max	Package			Page
8080-, SC/MP-Compatible	MP20	8 differential 16 single-ended	8 bits	±0.8, high ±0.4, low	±40	QIP			6-205
6800-, 6502-Compatible	MP21	8 differential 16 single-ended	8 bits	±0.8, high ±0.4, low	±40	QIP			6-217
Universal	MP22BG	8 differential 16 single-ended	12 bits	±0.4, high ±0.1, low	±25(1)	QIP			6-229
High-Accuracy	MP32BG MP32CG	8 differential 16 single-ended	12 bits 12 bits	±0.05 ±0.025	±60 ±60	QIP QIP			6-237 6-237

MICROPROCESSOR INTERFACED ANALOG OUTPUT SYSTEMS

Description	Model	Channels	Resolution	Accuracy (% of FSR) max	Tempco (ppm/°C) max	Package			Page
8080-, SC/MP-Compatible	MP10	2	8 bits	±0.4	±80	Ceramic 32-pin DIP			6-197
6800-, 6502-Compatible	MP11	2	8 bits	±0.4	±80	Ceramic 32-pinDIP			6-197

NOTES: 1) Unipolar, excluding IA.

SAMPLE/HOLD CIRCUITS

Proven technologies applied to these circuits achieve very high speed and accuracy for demanding applications. SHC298AM is a low cost monolithic. Designed to be performance compatible to Burr-Brown A/D and D/A converters, the application of all of these S/H circuits is quick and easy.

SAMPLE/HOLD CIRCUITS

Description	Model(1)	Gain/Offset Error (%) (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)(2)	Package			Page
Low Cost, Complete	SHC80KP	±0.01, ±2 max	±2 max	0.5 max	3	10 max	DIP			6-342
High Speed, Complete	SHC85, (Q) SHC85ET, (Q)	±0.01, ±2 max ±0.01, ±2 max	±2 max ±2 max	0.5 max 0.5 max	3 3	4.5 max 4.5 max	DIP(3) DIP(3)			6-346 6-346
Low Cost, Monolithic	SHC298AM	±0.01, ±7 max	±25 max	**0.2 max(4)**	4	10 max	TO-99(3)			6-350
Very-High Speed	SHM60	±0.01, ±1.5	±1.5	5	2	1 max	Module			6-356

NOTES: 1) "(Q)" indicates product also available with screening for increased reliability. See Q Program, page x. 2) 10V steps to 0.01% of final value. 3) Hermetic. 4) With 1000pF external holding capacitor.

MULTIPLEXERS

Models MPC4, MPC8 and MPC16 offer over-voltage protected inputs that can withstand up to 20 volts greater than either supply - especially important when input signals are present and MUX power is off. Models MPC800 and MPC801 provide fast settling time for high throughput rate systems. All models have internal channel selection decoding and low leakage current to be compatible with higher accuracy systems.

MULTIPLEXERS

Description	Model	Channels	Input Range (V)	On Resistance max	Crosstalk (% of OFF Channel Signal)	Settling Time (to 0.01%)	Package			Page
Protected Inputs	MPC8S	8 single	±15	1.8kΩ	0.005	5μsec	DIP			6-267
	MPC4D	4 differential	±15	1.8kΩ	0.005	5μsec	DIP			6-267
	MPC16S	16 single	±15	1.8kΩ	0.005	7μsec	DIP			6-274
	MPC8D	8 differential	±15	1.8kΩ	0.005	7μsec	DIP			6-274
High Speed	MPC800KG	16 single or	±15	750Ω	0.004	800nsec	DIP			6-253
	MPC800SG	8 differential	±15	750Ω	0.004	800nsec	DIP			6-253
	MPC801KG	8 single or	±15	750Ω	0.004	800nsec	DIP			6-260
	MPC801SG	4 differential	±15	750Ω	0.004	800nsec	DIP			6-260

SPECIAL PRODUCTS

We offer high performance products created specifically to meet unusual and extremely demanding application requirements. Among these products are wide temperature converters (see pages xiii and xv) and amplifiers (pages iii and vi) specified to operate over −55°C to +200°C.

For digital-audio applications we offer PCM-Audio Converters. PCM50 and PCM75 converters provide low distortion and high speed. They are the first converters with specified THD! Both are compatible with EIAJ STC-007 specifications.

PCM ANALOG-TO-DIGITAL CONVERTERS FOR AUDIO								
Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Conversion Time (max)	Input Range (V)	Temp Range[1]	Dynamic Range	Page
PCM-Audio A/D Converter[1]	PCM75KG	16	0.02% at −15dB	17μsec[2]	±2.5, ±5, ±10	Com	90dB	6-298
	PCM75JG	14[4]	0.05% at −15dB	15μsec[2]	±2.5, ±5, ±10	Com	90dB	6-298
PCM DIGITAL-TO-ANALOG CONVERTERS FOR AUDIO								
Description	Model	Resolution (Bits)	Total Harmonic Distortion (max)	Settling Time	Output Range (V)	Temp Range[1]	Dynamic Range	Page
PCM-Audio D/A Converter	PCM50KG	16	0.02% at −15dB	5μsec	±10, ±5	Com	96dB	6-281
	PCM52JG-V	**16**	**0.02% at F.S.**	**3μsec**	**±5**	**Com**	**96dB**	**93**
	PCM53JG-V	**16**	**0.02% at F.S.**	**3μsec**	**±10**	**Com**	**96dB**	**93**

NOTES: 1) Com = 0 to +70°C. 2) Can be reduced to 8μsec. 3) Internal 16-bit DAC available to user. 4) Can be operated at 16 bits.

Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

MILITARY PRODUCTS

Burr-Brown's Military Products meet the demands for high quality products for high reliability applications. They feature exceptional electrical performance from −55°C to +125°C, Hi-Rel manufacture, MIL-STD-883 class B screening, and reasonable prices.

They are designed to conservative and stringent MIL-M-38510 requirements, and are produced on a separate manufacturing line, which exceeds Burr-Brown's standard lines' quality. MIL-M-38510 and MIL-STD-883 processes and controls are used throughout. Cleanliness is impeccable, and the particle count in the assembly area is reduced by filtered, laminar air flow. The internal visual inspection is per method 2010 or 2017 and is performed three times. A monometallic wirebond system is used and anti-static precautions (including ion grids) and atmospheric moisture are constantly observed.

Complete, 12- to 16-page Detailed Specifications (data sheets) are written in MIL-M-38510 format and contain the information necessary for non-standard parts approval by the procuring activity on government programs. They contain fully specified min and max parameters, tests performed, MIL-STD-883 class B screening and burn-in, qualification and quality conformance inspections, and life testing. Applications information and typical performance are included in most Detailed Specifications.

Applications for Burr-Brown's Military Products range from critical applications, such as a missile or tactical weapon, to routine applications, such as signal processing or test equipment. Three electrical performance grades (U, V, and W) and three product assurance levels (standard, /883B, and /MIL) within each product series provide a performance/product assurance choice for each application.

/MIL PROCESSING

Sequence	Method	Requirements*
Manufacture		Burr-Brown high reliability manufacture includes traceability, rework and rebonding provisions, product and process change controls, date coding, etc.
Screening (Class B)	MIL-STD-883 Method 5004	Class B, 100% • Internal visual (Method 2010/2017) • Stabilization bake • Temperature cycle • Hermeticity, fine leak • Hermeticity, gross leak • Interim electrical • Burn-in • Constant acceleration • Final electrical • External visual
Qualification Conformance Inspection	MIL-STD-883 Method 5005/5008	Groups A & B plus periodic groups C & D • Group A - electrical tests • Group B - mechanical tests • Group C - die-related tests • Group D - package related tests
Qualification	MIL-STD-883 Method 5005/5008	Groups A, B, C & D upon special request (Most recent data available)

*See the detailed product data sheet for each product.

ANALOG-TO-DIGITAL CONVERTERS								
Model	Resolution Bits	Linearity ±LSB, max	Conversion Time μsec, max	Gain Drift ±ppm/°C, max	Input Range V	Temperature Range	Package	Page
ADC87/MIL[1]	12	1/2	8	15	±2.5,	MIL	32-pin DIP	7-7
ADC87/883B	12	1/2	8	15	±5,	MIL		7-7
ADC87	12	1/2	8	15	±10,	MIL		7-7
ADC87U/883B	12	1/2	8	15	0 to +5,	MIL		7-7
ADC87U	12	1/2	8	15	0 to +10	MIL		7-7

DIGITAL-TO-ANALOG CONVERTERS

Model	Resolution Bits	Linearity ±LSB, max	Monotonicity	Gain Drift ±ppm/°C, max	Settling Time max	Output Ranges	Temperature Range	Package		Page
DAC87-CBI-V/MIL	12	1/2	-55°C/+125°C	20	7	±2.5,	MIL			7-23
DAC87-CBI-V/B	12	1/2	-55°C/+125°C	20	7	±5,	MIL	24-pin		7-23
DAC87-CBI-V	12	1/2	-55°C/+125°C	20	7	±10,	MIL	DIP		7-23
DAC87U-CBI-V/B	12	1/2	-25°C/+85°C	20	7	+5,	MIL			7-23
DAC87U-CBI-V	12	1/2	-25°C/+85°C	20	7	+10	MIL			7-23

VOLTAGE-TO-FREQUENCY CONVERTERS

Model	V_{IN} Range V	F_{OUT} Range kHz, max	Linearity % FSR, max	Full Scale Drift ppm FSR/°C, max	Temperature Range	Package		Page
VFC32WM/883B	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100		7-61
VFC32WM	±10	200	±0.006 at 10kHz	±100 at 10kHz	MIL	TO-100		7-61
VFC32VM/MIL	±10	200	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100		7-61
VFC32VM/883B	±10	200	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100		7-61
VFC32VM	±10	200	±0.01 at 10kHz	-400, +150 at 200kHz	MIL	TO-100		7-61
VFC32UM/883B	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100		7-61
VFC32UM	±10	200	±0.01 at 10kHz	±150 at 10kHz	MIL	TO-100		7-61

MULTIPLIERS

Model	Accuracy at 25°C ±%, max	Accuracy at 125°C ±%, max	Feedthrough ±mV, max	Output Offset ±mV, max	Output V, mA, min	Temperature Range	Package		Page
4213WM/883B	1/2	4	50	25		MIL	TO-100		7-92
4213WM	1/2	4	50	25		MIL	TO-100		7-92
4213VM/MIL	1	4	100	30		MIL	TO-100		7-92
4213VM/883B	1	4	100	30	±10, ±5	MIL	TO-100		7-92
4213VM	1	4	100	30		MIL	TO-100		7-92
4213UM/883B	1	2*	100	50		MIL	TO-100		7-92
4213UM	1	2*	100	50		MIL	TO-100		7-92

*at +85°C.

OPERATIONAL AMPLIFIERS

Description	Model	Offset Voltage at 25°C ±mV, max	Offset Voltage drift ±μV/°C max	Bias Current nA, max	Bandwidth Unity Gain MHz, min	Slew Rate V/μs, min	ts ±0.01% ns	Compen-sation	Output V, mA, min	Temp. Range	Package		Page
Wideband	OPA600VM/MIL	4	20	−100pA		400	125			MIL			7-45
	OPA600VM/883B	4	20	−100pA		400	125			MIL	16-pin		7-45
	OPA600VM	4	20	−100pA	5000, ǂ, A = 1000	400	125	external	±10, ±200	MIL	DIP		7-45
	OPA600UM/883B	5	80	−100pA		400	150			MIL			7-45
	OPA600UM	5	80	−100pA		400	150			MIL			7-45
General Purpose Bipolar	3500R/MIL	5	20	±30	1	0.6	—			MIL			7-73
	3500R/883B	5	20	±30	1	0.6	—	internal	±10, ±10,	MIL	TO-99		7-73
	3500U/883B	5	20*	±30	1	0.6	—			MIL			7-73
Precision Bipolar	3510VM/MIL	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99		7-84
	3510VM/883B	0.12	2	±25	0.25	0.5	—	internal	±10, ±10	MIL	TO-99		7-84
Low Drift, Low Bias	OPA105WM/MIL	0.250	2	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105WM/883B	0.250	2	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105WM	0.250	2	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105VM/MIL	0.250	5	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105VM/883B	0.250	5	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105VM	0.250	5	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105UM/883B	0.250	15*	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
	OPA105UM	0.250	15*	−1pA	1	**0.9**	—	internal	±10, ±10	MIL	TO-99		7-35
Ultra Low Bias Current	**OPA106WM/MIL**	**0.250**	**5**	**−100fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106WM/883B	**0.250**	**5**	**−100fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106WM	**0.250**	**5**	**−100fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106VM/MIL	**0.250**	**10**	**−150fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106VM/883B	**0.250**	**10**	**−150fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106VM	**0.250**	**10**	**−150fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106UM/883B	**0.250**	**20***	**−300fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**
	OPA106UM	**0.250**	**20***	**−300fA**	**1**	**1.2**	—	**internal**	**±10, ±5**	**MIL**	**TO-99**		**117**

ǂ Gain-bandwidth product. * −25°C/+85°C.

NOTES: 1) ADC87/MIL available in the 4th quarter of 1983.

MODULAR POWER SUPPLIES

A broad line of compact, easily mounted encapsulated power supplies, AC/DC and DC/DC converters, are available from Burr-Brown. They are designed to power analog interface circuitry involving operational, instrumentation and isolation amplifiers, A/D and D/A converters and analog circuit functions in digital and analog systems: DC/DC converters offer high input-output isolation for those computer interface applications where analog circuitry must be floated independent of digital ground.

We provide a wide range of output voltages and current. International input voltage ratings are also available.

AC/DC CONVERTERS

Description	Model	Rated Output	Rated Input	Regulation No Load to Full Load	Regulation Overrated Line Volt	Output[1] Ripple/Noise	Package			Page
Dual ±15VDC Supply P.C.B. Mount	550	±15V, ±25mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	2mV	Module			8-3
	551	±15V, ±50mA		±0.05%	±0.05%	0.5mV	Module			8-3
	552	±15V, ±100mA		±0.05%	±0.05%	0.5mV	Module			8-3
	553	±15V, ±200mA		±0.05%	±0.05%	0.5mV	Module			8-3
	554	±15V, ±350mA		±0.02%	±0.02%	0.5mV	Module			8-3
Dual ±15VDC Supply Chassis Mount	556	±15V, ±200mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.05%	±0.05%	1mV	Module			8-3
	558	±15V, ±500mA		±0.05%	±0.05%	1mV	Module			8-3
5VDC Supply P.C.B. Mount	560	5V[5], ±250mA	105VAC to 125VAC, 50Hz to 400Hz [2] [3] [4]	±0.1%	±0.05%	1mV	Module			8-3
	561	5V[5], ±500mA		±0.1%	±0.05%	1mV	Module			8-3
	562	5V[5], ±1000mA		±0.1%	±0.05%	1mV	Module			8-3

DC/DC CONVERTERS

Description	Model	Input	Output	Isolation	Leakage Current	Package			Page
Regulated	546	4.5VDC to 5.5VDC 400mA	Single-Bipolar ±15V, 120mA	300V	Not Specified	Module			8-3
Isolated	700	10VDC to 18VDC 89mA	±10VDC to ±18VDC ±1V tolerance at 60mA total	1500Vp	1μA, max	Module			8-7
	700U[6]	10VDC to 18VDC 89mA	±10VDC to ±18VDC ±1V tolerance at 60mA total	2000Vp	1μA, max	Module			8-7
	710[7]	10VDC to 18VDC 100mA	Four sets of outputs each set: ±10VDC to ±18VDC ±1V tolerance at 76mA total all outputs	1000Vp	1μA, max	Module			8-9
Isolated	722	5VDC to 16VDC 120mA	Two-Bipolar ±15V, 64mA	3500V[8]	1μA at 240V, 60Hz	DIP			8-13
	722BG			8000V[9]					8-13
	724	5VDC to 16VDC 125mA	Four-Bipolar ±8V	1000V[8] 3000V[9]	1μA at 240V, 60Hz	DIP			8-17

NOTES: 1) At full load, rms (max). 2) 205VAC, 50Hz to 400Hz option available. 3) 90VAC to 110VAC, 50Hz to 400Hz option available. 4) 220VAC to 260VAC, 50Hz to 400Hz option available. 5) Connect as +5V or −5V. 6) Models 700 and 700M have separate internal input and output shields. Models 700U and 700UM have no internal shields. Model 700M and 700UM are similar to Models 700/700U but, in addition, they are 100% screened to patient connected circuit requirements for the leakage current (par. 27.5) and withstand voltage (par. 31.11) of UL544. Additional charge for 700M or 700UM. See Product Data Sheet for complete specifications. 7) Model 710 provides 4 channels (sets) of isolated outputs. See Product Data Sheet for complete specifications. 8) Input to output, 5sec, minimum.

DATA ENTRY AND DISPLAY TERMINALS

MICROTERMINAL™

If your system's data entry/control/display requirements are sophisticated, but limited in volume, you don't need to buy big, expensive and fragile CRT's or printing terminals to do the job efficiently.

"Microterminal™" is uniquely flexible in application versatility and is designed expressly to fill the human interface demands of widely dispersed control and communications networks - in machine and process control, energy management systems, inventory control and factory floor data collection and information processing systems. Microterminal™, because of its interface flexibility, appearance, size, durability and easy installation, functions equally well as consoles and control centers for instruments and small systems. It also performs as I/O terminals in diagnostic applications.

Tough, water-resistant front panel protects LED displays and indicators as well as keyboard. Tactile feedback confirms operator entry.

Buffered data features reduce on-line input/output time with the CPU and improve accuracy of operator inputs. And, because of its design simplicity, the Microterminal™ concept doesn't require special operator skills or training. Depressing a single function key initiates complex preprogrammed action by the CPU. These functions are defined in your CPU's software.

Microterminal™ offers very compact design and simple mounting on any flat surface, making it quickly adaptable to new or existing applications. It measures only 216mm × 114mm × 15mm (8.5" × 4.5" × 0.6"). When ordered in OEM quantities the front panel can contain your corporate or system logo.

MICROTERMINALS										
	LOW COST		GENERAL PURPOSE				DIGITAL I/O		BAR CODE READER[7]	
MODEL NUMBER	TM25 -300-XX	TM27	TM70	TM76/ TM76K	TM71	TM77/ TM77K	TM71 -I/O	TM77 -I/O	TM71B -XX	TM77B -XX
DISPLAY TYPE[1]	HEX	HEX	A/N	A/N	A/N	A/N	A/N	A/N	A/N	A/N
NUMBER OF CHARACTERS IN DISPLAY	8	8	12	12	16	16	16	16	16	16
INTERNAL BUFFER SIZE (INPUT AND OUTPUT)	8	8	36	36	80	80	80	80	80	80
KEYPAD TYPE[1]	HEX & NUM	HEX or NUM	A/N	NUM[5]	A/N	NUM[5]	A/N	NUM	A/N	NUM
DATA TRANSMISSION[2] (NONPOLLED MODE)	BLOCK	BLOCK	ECHO	ECHO	BLOCK	BLOCK	BLOCK	BLOCK	BLOCK	BLOCK
COMMUNICATION INTERFACE[3]	RS232 & C/L	RS422 or RS232	RS232 & C/L	RS232 & C/L	RS232 & C/L or RS422	same as TM71	same as TM71	same as TM71	RS232 or C/L RS422	same as TM71B
MULTIDROP CAPACITY	8	63	15	15	15 or 63	15 or 63	15 or 63	15 or 63	63	63
FUNCTION KEYS[4]	7	6	8	8	14	14	14	14	16	16
BAUD RATE	300	300 to 4800[8]	300 & 1200	300 & 1200	110 to 19,200	110 to 19,200	110 to 19,200	110 to 19,200	110 to 19,200	110 to 19,200
DIGITAL INPUTS	NO	3	NO	NO	NO	NO	NO[6]	NO[6]	NO	NO
DIGITAL OUTPUTS w/LED's	NO	5	2	2	2	2	2[6]	2[6]	2	2
USER EPROM	NO	NO	NO	NO	YES	YES	YES	YES	NO	NO
8-BIT I/O PORT — OUTPUT w/LED's	NO	NO	NO	NO	NO	NO	YES	YES	NO	NO
8-BIT I/O PORT — BIDIRECTIONAL	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
POWER SUPPLY	15VDC	8-12VDC voltage regulator	5VDC	5VDC	5VDC	5VDC	5VDC	5VDC	5VDC or 20-30 VDC + 15-28 VAC	same as TM71B
PAGE	9-5	9-19	9-27	9-27	9-42	9-42	9-42	9-42	9-60	9-60

NOTES: 1) A/N = Alphanumeric, HEX = Hexadecimal, NUM = Numeric. 2) In ECHO mode each character is sent upon key press. In BLOCK mode the entire line is sent when ENTER key is pressed; no echo is needed. 3) C/L = Current Loop with optical isolation. For TM71, 77, 71-I/O, and 77-I/O add "-21" for RS-422. No suffix for RS-232 and C/L. 4) On all but TM25, the function keys can be reprogrammed. 5) "K" models feature gasketed keyboards with plastic keycaps. 6) The TM71-I/O and 77-I/O have 8-bit I/O ports. 7) Re: Two digit suffix "-XX". The first digit designates communication interface: (1) RS-232, (2) RS-422. The second digit is for power supply: (1) 5VDC, (2) 20-30VDC and 15VAC. 8) 300, 1200, 2400, 4800.

MICROCOMPUTER I/O SYSTEMS

This full line of μC compatible I/O boards is available off-the-shelf. Design features let you put your microcomputer-based system together fast, using these analog and digital I/O's that offer: simple software requirements; memory-mapped designs; up to 64 input channels per board; analog inputs and outputs on the same board; 9-or 12-bit resolutions; software programmable gains; relay outputs; isolated digital I/O. Plug compatible with Intel, DEC, National, Motorola, Rockwell, Zilog, Synertek, AMC and others.

MULTIBUS™ ANALOG I/O									
Model	Analog Input	Analog Output	Inputs High Level	Inputs Low Level	Analog Resolution (bits)	Number Channels Input	Number Channels Output	Features	Page
MP8304		•	•		12		4	Individual D/A converters	10-29
MP8305		•	•		12		4	MP8304 without cable	10-29
MP8316-V		•	•		12		16	Low cost per channel	10-33
MP8316-I		•			12		16	4 to 20mA inputs	10-33
MP8418	•		•	•	12	15 DIF/31 SE		Resistor programmable gain	10-35
MP8418-AO	•	•	•	•	12	15 DIF/31 SE	2	Resistor programmable gain	10-35
MP8418-PGA	•		•	•	12	15 DIF/31 SE		Software programmable gain	10-35
MP8418-PGA-AO	•	•	•	•	12	15 DIF/31 SE	2	Software programmable gain	10-35
MP8418-EXP	(1)		(1)	(1)	(1)	48 DIF/96 SE		Analog input expander	10-39
MP8418-ISOE	(1)		(1)	(1)	(1)	**16 DIF**		**400V isolation [relay]**	**137**
MP8430	•		•	•	**12**	**16 DIF**		**RTD excitation, line length comp.**	**142**
MP8450	•		•	•	**12**	**16 DIF**		**1000V isolation [solid state]**	**146**
MP8608	•		•	•	8	8 DIF		Low cost	10-41
MP8608-AO	•	•	•	•	8	8 DIF	2	Low cost	10-41
MP8616	•		•	•	8	16 SE		Low cost	10-41
MP8616-AO	•	•	•	•	8	16 SE	2	Low cost	10-41
MP8632	•		•	•	8	32 DIF/64 SE		Low cost	10-41
MP8632-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost	10-41

MULTIBUS™ DIGITAL I/O						
Model	Digital Input	Digital Output	Number Channels	Isolated	Features	Page
MP801		•	16	•	Relay output	10-6
MP802		•	32	•	Relay output	10-6
MP810	•		**24**	•	**Contact closure input**	**129**
MP810-NS	•		**24**	•	**Voltage input**	**129**
MP810-LV	•		**24**	•	**Low voltage inputs**	**129**
MP810-AC	•		**24**	•	**AC sense inputs**	**129**
MP810-DB	•		**24**	•	**Contact closure, debounce circuit**	**129**
MP820-05	•		**5**	•	**Pulse count to 65,536**	**135**
MP820-15	•		**15**	•	**Pulse count to 65,536**	**135**
MP821-05	•		**5**	•	**Time measurement**	**135**
MP821-15	•		**15**	•	**Time measurement**	**135**
MP830-72	•		**72**		**TTL, Output read back**	**136**

MULTIBUS™ GENERAL PURPOSE CARDS		
Model	Description	Page
MP8510	**Multibus Extender Board**	**147**
MP8511	**Multibus Prototyping Board, holds 95 16-pin sockets, 2 50-pin I/O connectors**	**148**
MP8518	**Octal RS-232 Serial Interface, programmable baud rate from 50 to 19,200**	**149**
MP8519	**Quad RS-232 Serial Interface, programmable baud rate from 75 to 19,200**	**150**
MP8520	**32K-128K Dynamic RAM, 330nsec access time**	**151**
MP8525	**Intelligent Octal RS-232 Serial Interface, on-board processor**	**152**

NOTES: 1) Must be used with MP8418, MP8418-AO, MP8418-PGA or MP8418-PGA-AO which govern MP8418-EXP or MP8418-ISOE performance.

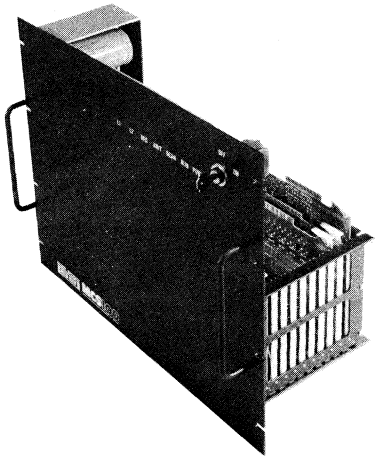
Models and page numbers in **bold type** are found in this supplement; others are in the Product Data Book.

MOTOROLA MICROMODULES ANALOG I/O										
Model	Analog Input	Analog Output	Inputs High Level	Inputs Low Level	Analog Resolution (bits)	Number Channels Input	Number Channels Output	Features		Page
MP7104		•			12		4	General purpose		10-17
MP7208	•		•	•	12	8 DIF/16 SE		General purpose		10-17
MP7216	•		•	•	12	8 DIF/16 SE		General purpose		10-17
MP7218	•		•	•	12	16 SE		Low cost		10-21
MP7408	•		•	•	8	8 DIF/16 SE		Low cost		10-23
MP7408-NS	•		•	•	8	8 DIF/16 SE		Low cost		10-23
MP7408-AO	•	•	•	•	8	8 DIF/16 SE	2	Low cost		10-23
MP7408-NS-AO	•	•	•	•	8	8 DIF/16 SE	2	Low cost		10-23
MP7432	•		•	•	8	32 DIF/64 SE		Low cost		10-23
MP7432-NS	•		•	•	8	32 DIF/64 SE		Low cost		10-23
MP7432-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost		10-23
MP7432-NS-AO	•	•	•	•	8	32 DIF/64 SE	2	Low cost		10-23
MP7504		•			8		4	Isolated-fused outputs		10-25
MP7608	•		•	•	12	8 DIF		200VDC protection		10-27
MP7608-1	•		•		12	8 DIF		Fused inputs		10-27

MOTOROLA MICROMODULES DIGITAL I/O							
Model	Digital Input	Digital Output	Number Channels	Isolated	Features		Page
MP701		•	16	•	Reed relays		10-2
MP702		•	32	•	Reed relays		10-2
MP710	•		24	•	Dry contact closures		10-4
MP710-NS	•		24	•	Voltage Input		10-4

DEC Q-BUS ANALOG I/O										
Model	Analog Input	Analog Output	Inputs High Level	Inputs Low Level	Analog Resolution (bits)	Number Channels Input	Number Channels Output	Features		Page
MP1104		•			12		4	Individual D/A converters		10-10
MP1216	•		•	•	12	32 SE		Resistor programmable gain		10-12
MP1216-PGA	•		•	•	12	32 SE		Software programmable gain		10-12
ZILOG MCB ANALOG I/O										
MP2216	•		•	•	12	32SE		Resistor programmable gain		10-15
MP2216-A0	•	•	•	•	12	32SE	2	Resistor programmable gain		10-15

REGULATED BATTERY-BACKED POWER SUPPLY							
Model	Rated Output	Output Ripple	Current Limit	Rated Input	Features		Page
PSB100	**+5VDC, 11.2A** **+12VDC, 1.2 A** **−12VDC, 1.2 A** **−5VDC, 100mA**	**150mV, p−p** **360mV, p−p** **360mV, p−p** **40mV, p−p**	**12.0A ±5%** **1.5A ±5%** **1.5A ±5%** **None**	**100-130VAC or 200-260VAC**	**Designed for use with microcomputer systems such as Multibus™ system. Provides signals for line power loss, or low internal battery.**		**127**



MCS SERIES

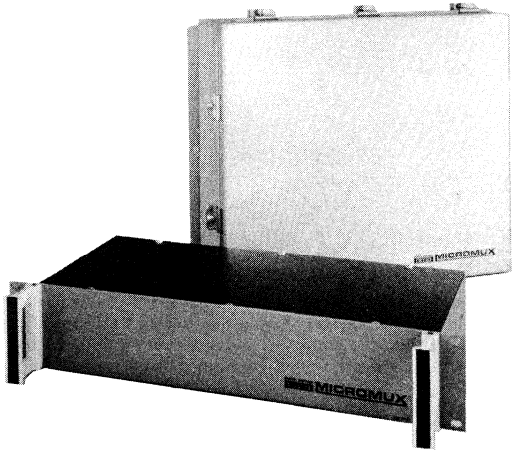
Truly Cost Effective Analog And Digital I/O

Low cost, Multibus ™ based data acquisition and control systems with 4 or 9 I/O cards. Screw terminations for all I/O, optional IEEE surge-withstand protection. MCS provides direct sensor interface for RTD's and thermocouples, with cold junction compensation and linearization. Voltage, current, discrete (TTL to 220VAC) I/O's; also isolated pulse inputs. Analog data may be scaled 0 to 100%. ASCII asynchronous serial interface; dual ports; multidroppable; RS-232, RS-422 and 20mA current loop. −10 to +60°C in NEMA or rack mount.

CS400 Series

A Stand-Alone Measurement And Control System That's Easy To Install, Program, Operate

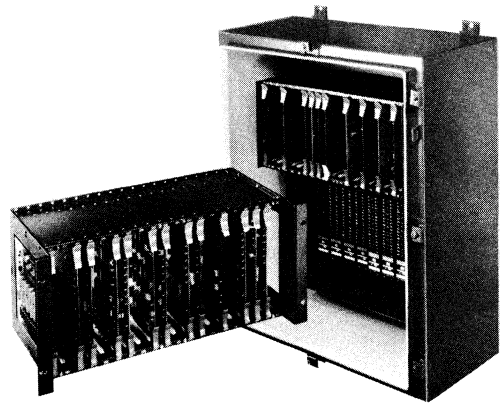
These measurement and control computers are easy to install and program using BASIC-400 or PASCAL. Includes a full line of Multibus™ process I/O with all driver software plus disk and/or digital tape storage, logging printer, and external Centronics printer interface and AUTOSTART capability. Optional 8-line serial I/O, RS-232 or current loop. Desk top or rack mount enclosure.



MICROMUX

A Two-Wire System That Takes The Cost And Complication Out Of Remote Data Acquisition

This two-wire remote input multiplexer puts NEMA 4 mounted, intrinsically safe transmitters near your sensors, accepting 16 analog or digital inputs each. Up to four transmitters connect to a receiver that interfaces asynchronously to the host (computer?) using serial ASCII characters, RS-232 or current loops. Eight multidrop receivers interface 512 intrinsically safe channels on one communications line!

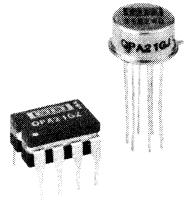


IOS2000

A Complete I/O System That Makes I/O Handling Easy . . . Reduces Control System Costs

Highly ruggedized remote data acquisition and control system. −40 to +85°C temp range, full autocalibration, extensive diagnostics and low power make IOS ideal for remote applications. IOS provides direct sensor interface for RTD's and thermocouples, with cold junction compensation and linearization. Voltage, current, discrete (TTL to 220VAC) I/O's; also isolated pulse inputs. Screw terminations for all I/O's. NEMA or rack mount.

BURR-BROWN®



OPA21

High-Speed Low-Power Precision OPERATIONAL AMPLIFIER

FEATURES

- LOW SUPPLY CURRENT
  230μA max at V_{CC} = ±15V
- HIGH SLEW RATE
  0.2V/μsec typ
- WIDE SUPPLY RANGE
  ±2.5V to ±18V
- LOW OFFSET VOLTAGE
  100μV max
- LOW OFFSET VOLTAGE DRIFT
  1.0μV/°C max
- HIGH CMRR AND PSRR
  110dB typ
- HIGH OPEN-LOOP GAIN
  120dB min

APPLICATIONS

- LOW POWER INSTRUMENTATION AMPLIFIERS
- ISOLATION AMPLIFIERS
- PORTABLE EQUIPMENT
- BATTERY OPERATION

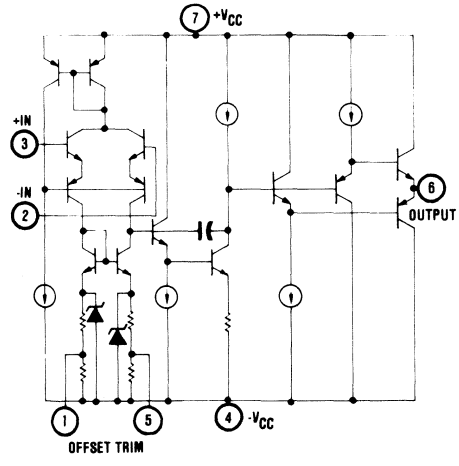
DESCRIPTION

A unique circuit design, state-of-the-art monolithic processing and advanced laser-trimming techniques are used to provide a low power amplifier with outstanding parameters - truly "instrumentation grade" performance.

The OPA21 maintains excellent performance features over a wide supply voltage range.

A maximum I_Q of 230μA means only 6.9mW of power consumption at the V_{CC} = ±15V and 1.1mW at V_{CC} = ±2.5V.

This design also has lower input bias and offset currents than other low power op amps. This is particularly important in low power applications where the high resistor values used can create large voltage errors due to bias current. The OPA21 is internally compensated and has excellent frequency stability characteristics.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 2.5VDC to 15VDC unless otherwise noted.

PARAMETERS	CONDITIONS	OPA21A, OPA21E			OPA21B, OPA21F			OPA21G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INITIAL OFFSET VOLTAGE ($\pm V_{CC}$ = 15VDC)											
Initial Offset(1)			40	100		150	200		300	500	µV
Over Temperature(2)			75	200		200	500		500	1000	µV
Average vs Temperature(2)			0.5	1.0		1.0	2.0		2.5	5.0	µV/°C
Offset Adjustment Range			±4			•			•		mV
INPUT OFFSET CURRENT											
Initial Offset			0.3	1		0.8	2		1.2	4	nA
Over Temperature(2)			0.5	2		2.0	4		2	6	nA
INPUT BIAS CURRENT											
Initial Bias			7	25		10	40		15	50	nA
Over Temperature(2)			9	40		12	60		18	75	nA
INPUT NOISE											
Voltage	0.1Hz to 10Hz		1.0			•			•		µV, p-p
Voltage Density	f_o = 1Hz		60			•			•		nV/√Hz
	f_o = 10Hz		20			•			•		nV/√Hz
	f_o = 100Hz		20			•			•		nV/√Hz
Current Density	f_o = 1Hz		0.7			•			•		pA/√Hz
	f_o = 10Hz		0.25			•			•		pA/√Hz
	f_o = 100Hz		0.07			•			•		pA/√Hz
INPUT RESISTANCE											
Differential			6			5			4		MΩ
Common-Mode			10^{10} || 2			•			•		Ω || pF
INPUT VOLTAGE RANGE ($\pm V_{CC}$ = 15VDC)											
Initial Input Voltage		-12.5			•			•			V
		+14.3			•			•			V
Over Temperature(2)		-12.0			•			•			V
		+14.0			•			•			V
COMMON-MODE REJECTION RATIO ($\pm V_{CC}$ = 15VDC, No Load, $-12 \leq V_{CM} \leq +14V$)											
Initial Rejection Ratio		100	110		90	105		84	100		dB
Over Temperature(2)		96	105		86	100		80	95		dB
POWER SUPPLY REJECTION RATIO ($\pm V_{CC}$ = 2.5V to 18V, No load											
Initial Rejection Ratio		104	114		100	108		90	100		dB
Over Temperature(2)		100	108		95	104		85	95		dB
LARGE SIGNAL VOLTAGE GAIN ($\pm V_{CC}$ = 15VDC, R_L = 10kΩ)											
Initial Voltage Gain		1000	2000		500	1500		500	1000		V/mV
		120	126		114	124		114	120		dB
Over Temperature(2)		500	1500		250	1300		250	1000		V/mV
		114	124		108	122		108	120		dB
RATED OUTPUT ($\pm V_{CC}$ = 15VDC, R_L = 10kΩ)											
Initial Voltage Swing		-13.7	-14.2		-13.7	•		-13.6	•		V
		+14.0	+14.1		+13.9	•		+13.8	•		V
Over Temperature(2)		-13.5			-13.5			-13.5			V
		+13.8			+13.7			+13.6			V
Output Resistance	Open-Loop		500			•			•		Ω
DYNAMIC RESPONSE											
Slew Rate	C_L = 100pF, R_L = 25kΩ		0.2			•			•		V/µsec
Closed-Loop Bandwidth	A_{CL} = +1, R_L = 10kΩ		300			•			•		kHz
POWER SUPPLY											
Rated Voltage			±15			•			•		VDC
Voltage Range		2.5		18	•		•	•		•	VDC
Current, Quiescent	No Load										
Initial	$\pm V_{CC}$ = 2.5V		(3)	210		•	225		•	250	µA
	$\pm V_{CC}$ = 15V		(3)	230		•	250		•	275	µA
Over Temperature(2)	$\pm V_{CC}$ = 2.5V		(3)	275		•	300		•	325	µA
	$\pm V_{CC}$ = 15V		(3)	325		•	350		•	375	µA
Power Consumption	$\pm V_{CC}$ = 15V, T_A = +25°C			6.9			7.5			8.3	mW
TEMPERATURE RANGE											
Specification A, B,		-55		+125	•		•	•		•	°C
E, F, G		-25		+85	•		•	•		•	°C
Operating A, B,		-55		+125	•		•	•		•	°C
E, F, G		-25		+85	•		•	•		•	°C
Storage	"J" and "Z" Packages	-65		+125	•		•	•		•	°C

*Specification same as OPA21A, OPA21E.

NOTES:

1. 100% tested. Guaranteed fully warmed-up. 2. Over temperature specifications are -55°C ≤ T_A ≤ +125°C for A and B grades and -25°C ≤ T_A ≤ +85°C for E, F, and G grades. 3. See Typical Performance Curves.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation(1) 500mW
Input Voltage ..... Supply Voltage
Differential Input Voltage ±30V
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range .... -65°C to +150°C
Operating Temperature Range
A, B, ... -55°C to +125°C
E, F, G ..... -25°C to +85°C
Lead Temperature Range
(Soldering, 60sec) ..... +300°C

NOTES:

1. Maximum package power dissipation vs ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	+80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	+75°C	6.7mW/°C

ORDERING INFORMATION

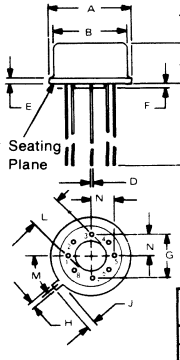
OPA21 Y Z

Basic Model Number
Performance Grade Code
A, B -55°C to +125°C
E, F, G -25°C to +85°C
Package Code
J TO-99
Z 8-Pin Hermetic DIP

TO-99 (J Suffix)	Hermetic DIP (Z Suffix)
OPA21AJ*	OPA21AZ*
OPA21BJ*	OPA21BZ*
OPA21EJ	OPA21EZ
OPA21FJ	OPA21FZ
OPA21GJ	OPA21GZ

*A and B grades available with MIL-STD-883 screening. To order add /833 as suffix to part number.

MECHANICAL



TO-99 PACKAGE
("J" SUFFIX)

NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

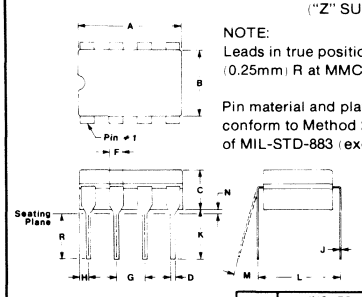
Pin numbers shown for reference only. Numbers may not be marked on package.

The TO-99 can and leads are bright acid tin plated.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.7	--
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

8-PIN HERMETIC DIP
("Z" SUFFIX)



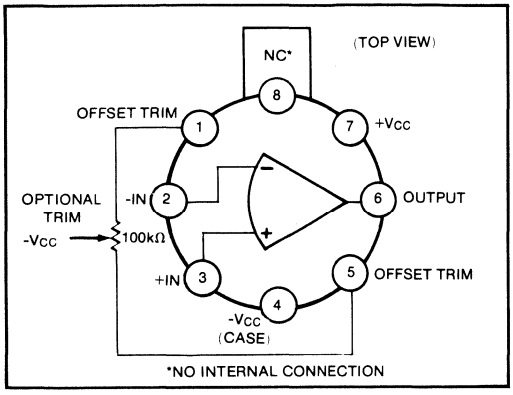
NOTE:
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

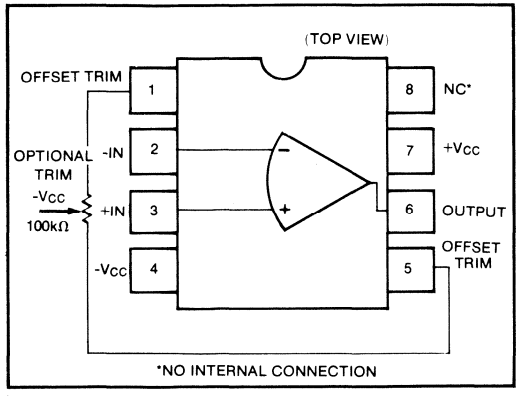
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.016	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	-	.098	-	2.49
J	.008	.012	0.20	0.30
K	.150	-	3.80	-
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

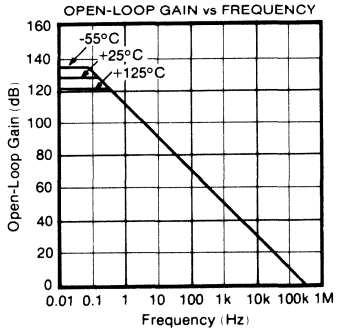
PIN CONFIGURATION

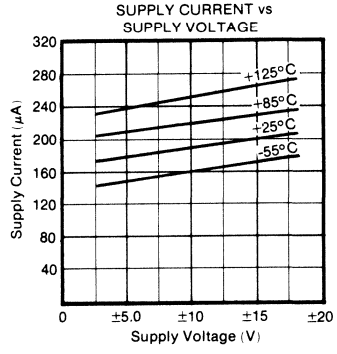


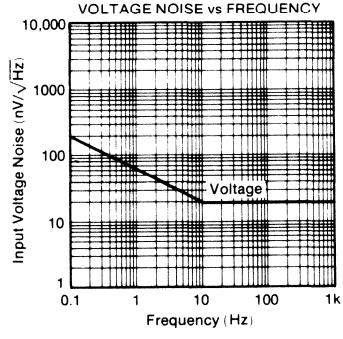


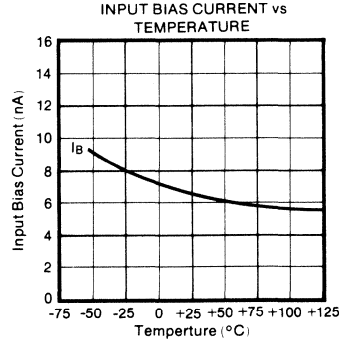
TYPICAL PERFORMANCE CURVES

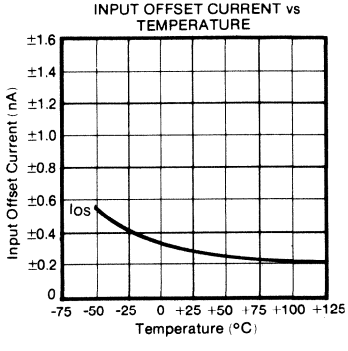
(T_A = +25°C, ±V_{CC} = 15VDC unless otherwise noted)

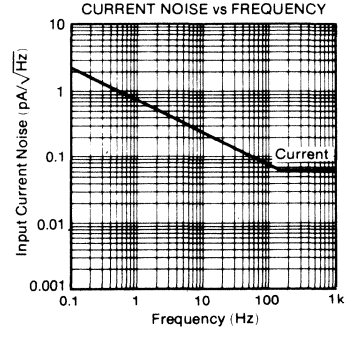












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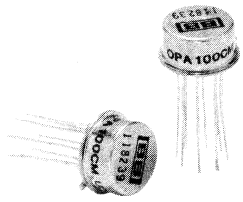


OPA100

Low Drift - Low Bias Current JFET Monolithic OPERATIONAL AMPLIFIER

FEATURES

- LOW INITIAL BIAS CURRENT
  1pA max at +25°C
- LOW BIAS CURRENT vs TEMPERATURE
  20pA max at +85°C
  40pA max at +125°C
- HIGH INPUT IMPEDANCE, $10^{12}\Omega$
- LOW OFFSET VOLTAGE, 250μV max
- LOW OFFSET VOLTAGE DRIFT, 5μV/°C max
- LOW NOISE, 20nV/$\sqrt{Hz}$ at 100Hz

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  pH electrodes
  Biological probes/transducers
- PHOTO DETECTOR CIRCUITS
- LONG-TERM PRECISION INTEGRATION
- HIGH IMPEDANCE BUFFER
- PRECISION SAMPLE/HOLD

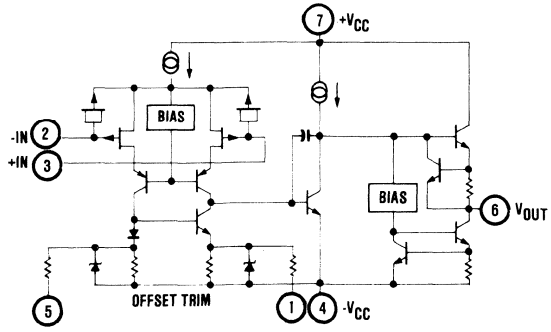
DESCRIPTION

The OPA100 is a precision monolithic low bias current operational amplifier. An enhanced bipolar FET process with JFET input transistors and dielectric isolation is used to achieve low input bias current. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation significantly reduces the bias current at higher temperatures.

Low offset voltage (250μV max) and low voltage drift (5μV/°C) are also guaranteed. This performance is achieved by active laser-trimming the amplifiers thin-film resistors. The OPA100 also produces low noise compared to other low bias current monolithic FET amplifiers.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to supply terminals without damage.

The standard pin configuration (741-type) of the OPA100 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA100AM/AG			OPA100BM,BG/SM,SG			OPA100CM/CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC	V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	T_A = +25°C	94	100		100	106		106	110		dB
	$T_A = T_{MIN}$ to T_{MAX}	88	100		94	106		100	110		dB
RATED OUTPUT											
Voltage at $R_L = 2k\Omega$	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		•	•		•	•		V
Current	$T_A = T_{MIN}$ to T_{MAX}	±5	±10		•	•		•	•		mA
Output Impedance			100			•			•		Ω
Load Capacitance[1]		500	1000		•	•		•	•		pF
Short Circuit Current		10	40		•	•		•	•		mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1			•			•		MHz
Full Power Response		10	32		•	•		•	•		kHz
Slew Rate		0.6	2		•	•		•	•		V/µsec
Settling Time 0.1%	10V step		6			•			•		µsec
Settling Time 0.01%	10V step		10			•			•		µsec
Overload Recovery, 50% overdrive[2]			5			•			•		µsec
INPUT OFFSET VOLTAGE[3]											
Initial Offset	T_A = +25°C		±200	±1000		±100	±500		±50	±250	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±15		•	±10		±1	±5	µV/°C
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}			±2			±1/±1.5			±0.5	mV
vs Supply	$T_A = T_{MIN}$ to T_{MAX}		±10	±100		•	±25		•	±25	µV/V
INPUT BIAS CURRENT[3]											
Initial Bias Current											
A, B, C Grades	T_A = +25°C		±1	±3		±0.6	±2		±0.3	±1	pA
S Grade	T_A = +25°C					±0.3	±1				pA
Over Temperature											
A, B, C Grades	T_A = +85°C		±10	±100		•	±40		±5	±20	pA
S Grade	T_A = +125°C					±10	±40				pA
INPUT OFFSET CURRENT											
Initial Difference Current	T_A = +25°C		±0.5			•			•		pA
Over Temperature											
A, B, C Grades	T_A = +85°C		±10			•			±5		pA
S Grade	T_A = +125°C					±10					pA
INPUT IMPEDANCE											
Differential			$10^{12} \parallel 6$			•			•		Ω || pF
Common-Mode			$10^{13} \parallel 6$			•			•		Ω || pF
INPUT NOISE											
Voltage, f_o = 10Hz			30			•			•		nV/√Hz
f_o = 100Hz			20			•			•		nV/√Hz
f_o = 1kHz			20			•			•		nV/√Hz
f_o = 10kHz			20			•			•		nV/√Hz
f_B = 0.1Hz to 10Hz			1			•			•		µV, p-p
Current, f_B = 0.1Hz to 10Hz			0.01			•			•		pA, p-p
f_B = 10Hz to 10kHz			0.03			•			•		pA, rms
f_o = 1kHz			0.6			•			•		fA/√Hz
INPUT VOLTAGE RANGE											
Differential		±18			•			•			V
Common-Mode	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		•	•		•	•		V
Common-Mode Rejection, $V_{IN} = \pm 10V$	$T_A = T_{MIN}$ to T_{MAX}	76	82		88	94		94	100		dB
Maximum Safe Input Voltage			±Vcc			•			•		V
POWER SUPPLY											
Rated Voltage			±15			•			•		VDC
Voltage Range, derated performance		±5		±18	•		•	•		•	VDC
Current, quiescent	$T_A = T_{MIN}$ to T_{MAX}		1.0	3		•	2		•	1.5	mA
TEMPERATURE RANGE	Ambient										
Specification											
A, B, C Grades		-25		+85	•		•	•		•	°C
S Grade		-55		+125	•		•	•		•	°C
Operating		-55		+125	•		•	•		•	°C
Storage		-65		+150	•		•	•		•	°C
θ junction-ambient			300			•			•		°C/W

*Specification same as for OPA100AM.

NOTES: 1. Stability guaranteed with load capacitance ≤ 500pF.
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive.
3. Offset voltage and bias current are guaranteed after 1 minute of operation at T_A = +25°C. They are 100% tested.

ORDERING INFORMATION

OPA100 X X

Basic model number

Performance grade
- A, B, C -25°C to +85°C
- S -55°C to +125°C

Package code
- TO-99 metal can, M
- 8-pin hermetic mini DIP, G

NOTE: MIL-STD-883 screening available. Add /883 to model number.

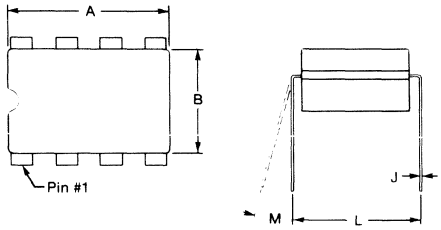
ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal power Dissipation(1)	500mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

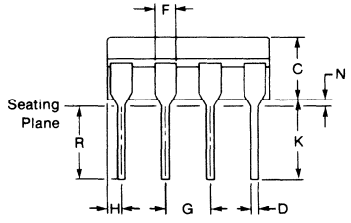
NOTES:
1. Package must be derated based on: θ_{JC} = 150°C/W or θ_{JA} = 300°C/W.
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common only. Rating applies to +25°C ambient.

MECHANICAL

8-PIN MINI DIP PACKAGE



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.



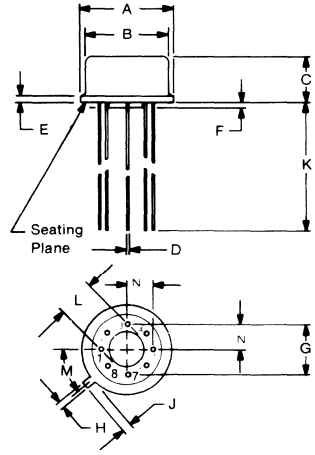
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.375	.405	9.53	10.28
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	-	.098	-	2.49
J	.008	.012	0.20	0.30
K	.150	-	3.80	-
L	.290	.320	7.37	8.13
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

TO-99 PACKAGE

NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

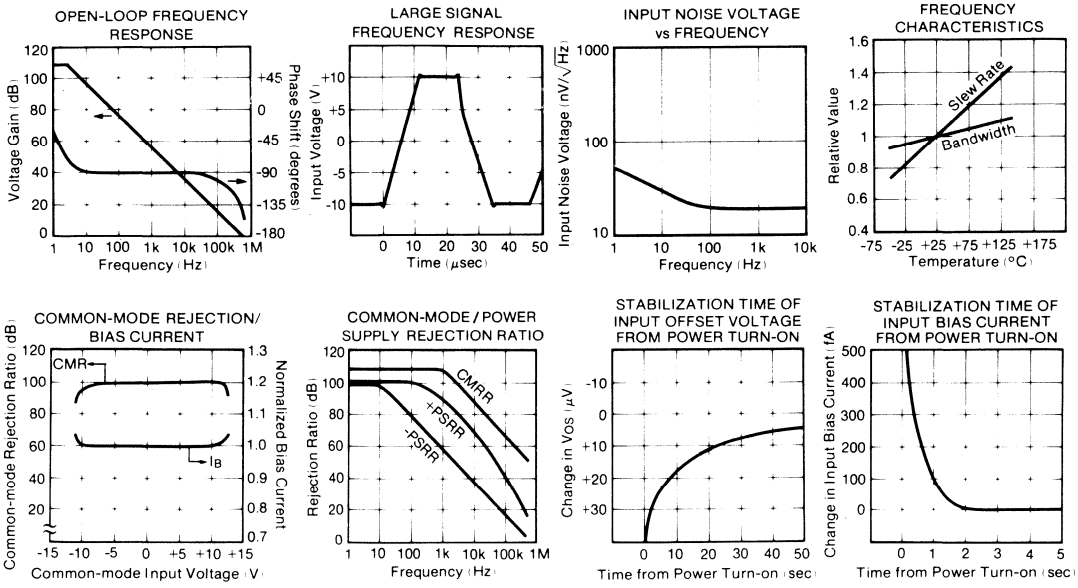
Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.



APPLICATIONS INFORMATION

INPUT BIAS CURRENT

The OPA100 uses FET input transistors with dielectric isolation to achieve low input bias currents. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation makes significant reduction in the bias current at higher temperatures. Figure 1 shows an improvement of over a decade for temperatures above +75°C.

The compensation causes the polarity of the bias current to be indeterminate (note the "±" signs for I_B in the electrical specifications). This means that the bias current may flow into or out of the amplifier inputs.

VOLTAGE NOISE

In many FET amplifier applications the voltage noise is a critical parameter. The bias current cancellation design of the OPA100 allows low noise without sacrificing low bias current. Figure 2 shows the noise of various types of

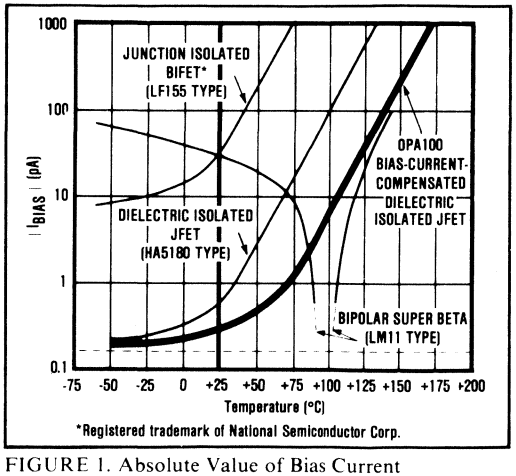


FIGURE 1. Absolute Value of Bias Current vs Temperature.

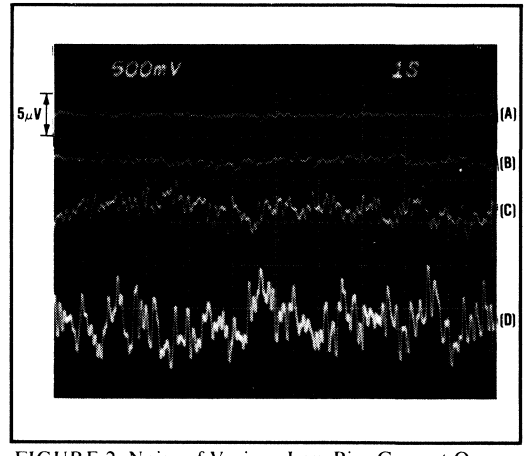


FIGURE 2. Noise of Various Low Bias Current Op Amps. (A) OPA100, (B) LF155 type, (C) LM11 type, (D) HA 5180 type.

low bias current operational amplifiers. The noise test circuit used has a gain of 100kV/V with a 1-pole filter at 0.1Hz and a 5-pole filter at 10Hz. It can be seen that the OPA100 has very-low noise when compared to other low bias current op amps.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA100. To avoid leakage problems, it is recommended that the signal input lead of the OPA100 be wired to a Teflon standoff. If the OPA100 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

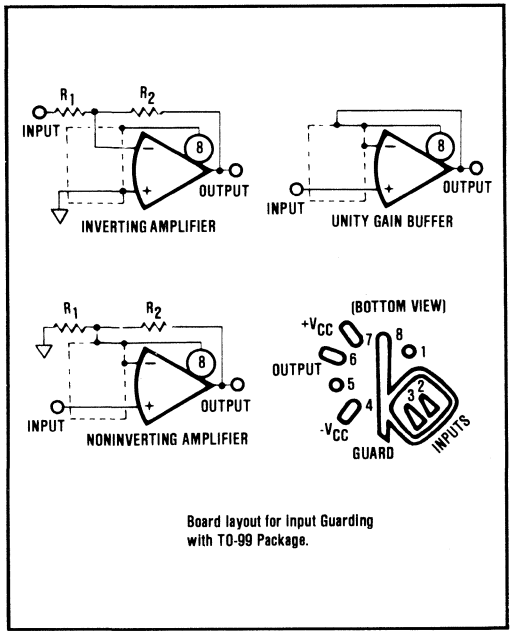


FIGURE 3. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA100 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. External offset voltage adjustment changes the drift by approximately 0.3μV/°C, for every 100μV of offset adjusted. See Figure 4.

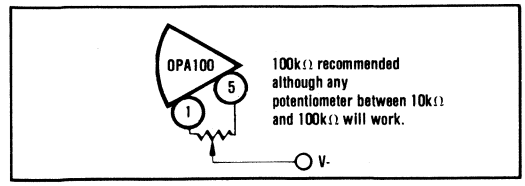


FIGURE 4. External Nulling of Offset Voltage.

APPLICATION CIRCUITS

The OPA100 is ideally suited for low bias current, high input impedance applications. Also because the noise and offset drift errors are low, total high performance can be achieved. Figures 5 through 8 show a photodiode, pH probe, isolation, and integrator amplifier.

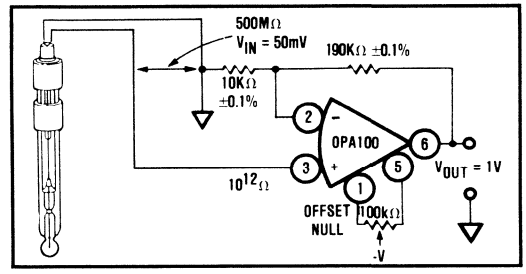


FIGURE 5. pH Probe Amplifier.

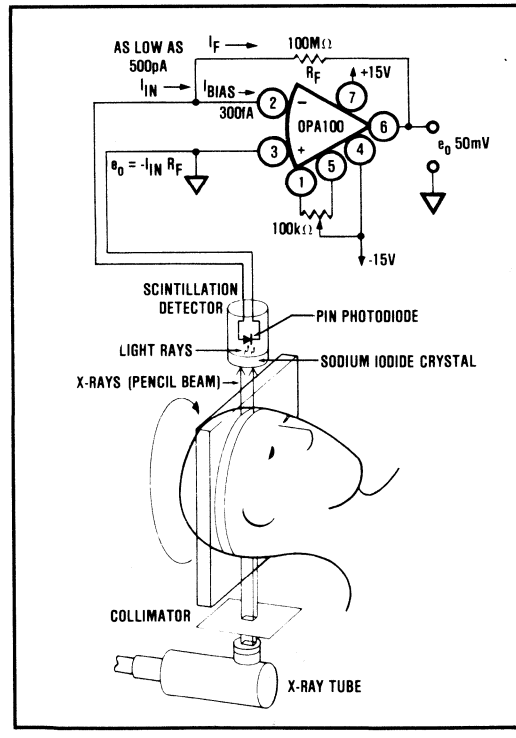


FIGURE 6. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

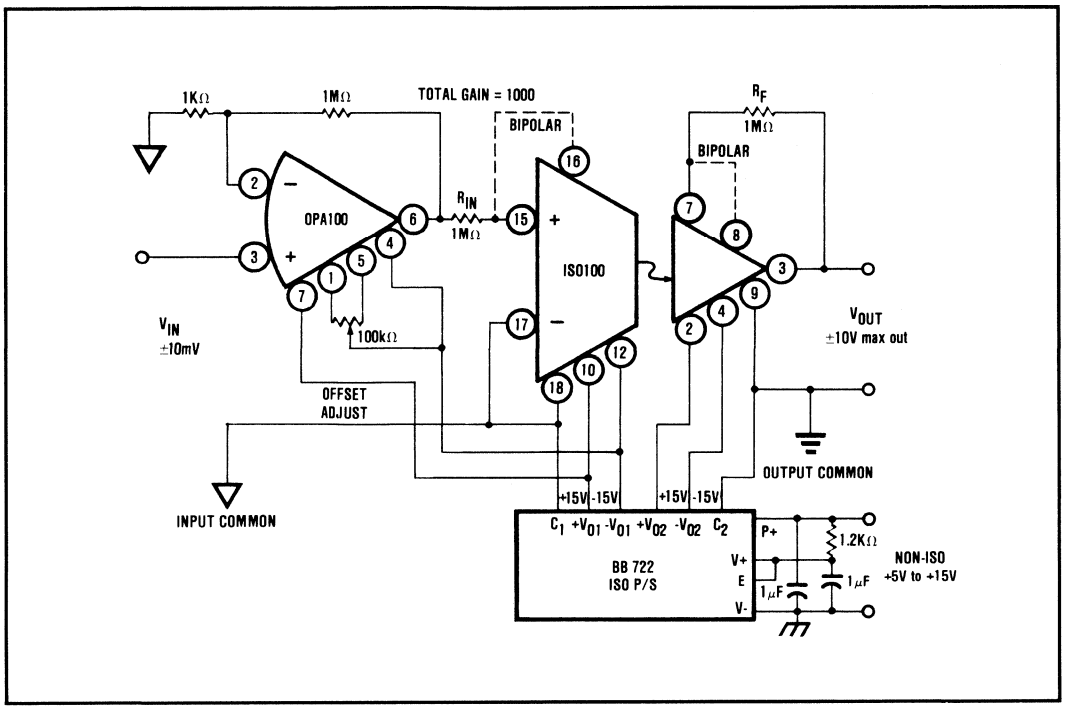


FIGURE 7. Low Level High Impedance Isolation Amplifier.

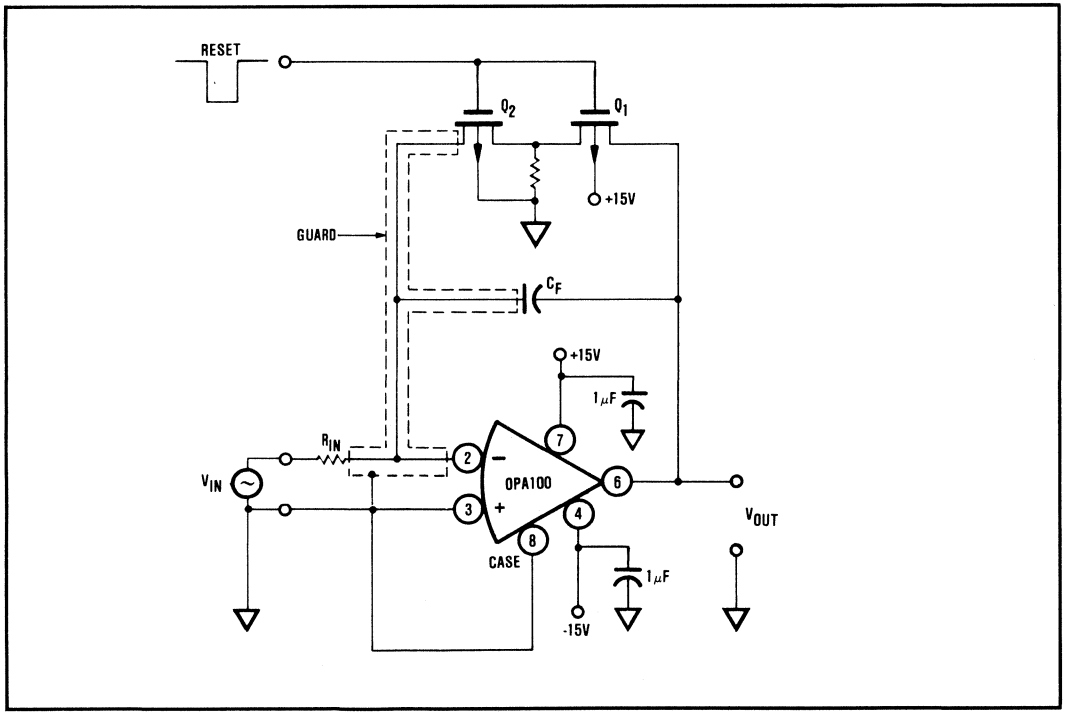
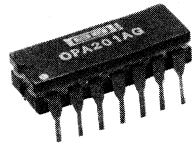


FIGURE 8. High Accuracy Integrator with Reset.

BURR-BROWN®

OPA201



PAT. PEND.

Switchable-Input Operational Amplifier SWOP AMP™

FEATURES

- TWO PRECISION INPUT STAGES SELECTABLE WITH CONTROL SIGNAL
- EXCELLENT INPUT SPECIFICATIONS
  - V_{OS} 100μV max (C Grade)
  - $\Delta V_{OS}/\Delta T$ 1μV/°C max (C Grade)
  - I_B 25nA max (C Grade)
- LOW POWER
  - $\pm V_{CC}$ 2.5V to 18V
  - I_Q 500μA max
- EASY TO USE

APPLICATIONS

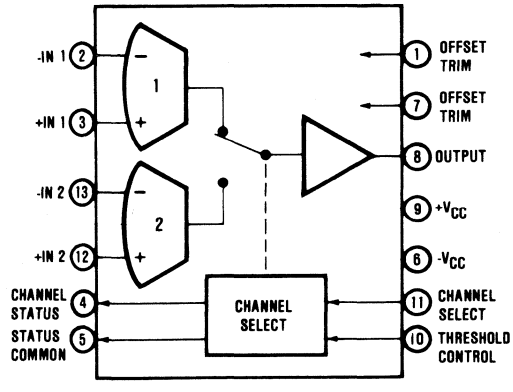
- AUTO-ZERO SYSTEMS
- TWO-CHANNEL MULTIPLEXER WITH GAIN
- SELECTABLE-INPUT INSTRUMENTATION AMPLIFIER
- SWITCHABLE-GAIN CIRCUITS
- SWITCHABLE-BANDWIDTH CIRCUITS
- SYNCHRONOUS MODULATOR/DEMODULATOR
- ISOLATION CIRCUITS
- BATTERY OPERATED SYSTEMS

DESCRIPTION

The OPA201 is a switchable-input operational amplifier (Swop Amp™). It contains two independent differential input stages and one output stage. Either of the input stages may be connected to the output stage under the control of the Channel Select digital input signal which is TTL-compatible or user-programmable. The OPA201 is easy to use and functions as an operational amplifier that can switch between two sets of inputs.

Each input stage provides excellent input characteristics: low offset voltage (100μV, max), low offset voltage drift versus temperature (1μV/°C, max), and low bias current (25nA, max).

Additionally, the Swop Amp is a low power device. It draws less than 500μA (max) over the supply range $\pm$2.5V to $\pm$18V. It is well suited for portable, remote, and other battery powered applications. Also, its low power consumption and excellent specifications make it well suited for isolation circuit applications. Burr-Brown's state-of-the-art monolithic design and processing, compatible thin-film resistors, and active laser trimming produce a truly unique highly versatile circuit. The unique switchable input stage design allows minimum hardware and minimum cost solutions to some very demanding analog circuit design problems.



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted. Specifications are for either channel 1 or 2 unless otherwise noted.

PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC	V_{OUT} = ±10V										
Rated Load, R_L = 10kΩ	T_A = +25°C	114	130		*	*		120	*		dB
	T_A = T_{MIN} to T_{MAX}	110			*			114			dB
RATED OUTPUT											
Voltage at R_L = 10kΩ	T_A = T_{MIN} to T_{MAX}	±13.5	±14		*	*		*	*		V
Current, V_{OUT} = ±10V			5			*			*		mA
Output Impedance			0.5			*			*		kΩ
Short Circuit Current			10			*			*		mA
INPUT OFFSET VOLTAGE[1]											
Either Channel											
Initial Offset[2]	T_A = +25°C		120	500		70	200		35	100	µV
Average Drift	T_A = T_{MIN} to T_{MAX}		1.4	5.0		0.9	2.0		0.5	1.0	µV/°C
Over Temperature[3]	T_A = T_{MIN} to T_{MAX}		150	1000		100	500		55	200	µV
vs Supply	$\pm V_{CC}$ = ±2.5V to ±18V										
	T_A = +25°C		8	32		5	18		4	10	µV/V
	T_A = T_{MIN} to T_{MAX}		10	60		6	32		5	16	µV/V
Match Between											
Channels 1 and 2											
Initial	T_A = +25°C		150	500		65	100		25	50	µV
Over Temperature[3]			150	1000		90	200		30	100	µV
INPUT BIAS CURRENT											
Initial Bias Current	T_A = +25°C		15	50		13	40		12	25	nA
Over Temperature[3]				60			50			30	nA
INPUT OFFSET CURRENT											
Initial Offset Current	T_A = +25°C		1.4	4		0.75	2		0.7	1	nA
Over Temperature[3]				6			4			2	nA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			500			*			*		kHz
Full Power Response			4			*			*		kHz
Slew Rate	T_A = T_{MIN} to T_{MAX}	0.1			*			*			V/µsec
Settling Time 0.1%	10V Step		49			*			*		µsec
Settling Time 0.01%	10V Step		52			*			*		µsec
INPUT IMPEDANCE											
Differential			6			*			*		MΩ
Common-Mode			10^{10} ‖ 2			*			*		Ω ‖ pF
INPUT NOISE											
Voltage	f_B = 0.1 to 10Hz		1			*			*		µV, p-p
Voltage Density	f_o = 1Hz		85			*			*		nV/√Hz
	f_o = 10Hz		27			*			*		nV/√Hz
	f_o = 100Hz		27			*			*		nV/√Hz
	f_o = 1kHz		27			*			*		nV/√Hz
Current	f_B = 0.1 to 10Hz		1.5			*			*		pA, p-p
Current Density	f_o = 1Hz		1000			*			*		fA/√Hz
	f_o = 10Hz		300			*			*		fA/√Hz
	f_o = 100Hz		100			*			*		fA/√Hz
	f_o = 1kHz		100			*			*		fA/√Hz
INPUT VOLTAGE RANGE											
Common-Mode	T_A = +25°C	−12.5		+12.5	*		*	*		*	V
Common-Mode	T_A = T_{MIN} to T_{MAX}	−12		+12	*		*	*		*	V
Common-Mode Rejection,	T_A = +25°C	85	94		90	98		95	98		V
V_{IN} = +10V	T_A = T_{MIN} to T_{MAX}	80	92		85	95		90	97		dB
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range,											
derated performance		±2.5		±18	*		*	*		*	VDC
Current, quiescent			425	500		*	*		*	*	µA
DIGITAL SIGNALS											
Threshold control											
(TC) Voltage Range		$-V_{CC}$		$+V_{CC}$ − 5	*		*	*		*	V
Channel Select (CSEL)[4]											
Voltage Range		$-V_{CC}$		$+V_{CC}$	*		*	*		*	V
V_{IH} (selects ch. 1)		V_{TC} + 2		$+V_{CC}$	*		*	*		*	V
V_{IL} (selects ch. 2)		$-V_{CC}$		V_{TC} + 0.8	*		*	*		*	V
	T_A = T_{MIN} to T_{MAX}	$-V_{CC}$		V_{TC} + 0.6	*		*	*		*	V
I_{IH}	V_{CSEL} = $+V_{CC}$		<1	50		*	*		*	*	µA
I_{IL}	V_{CSEL} = V_{TC} = 0V		25	60		*	*		*	*	µA
Status Common (SC)											
Voltage Range		$-V_{CC}$		[5]	*		*	*		*	V
Channel Status											
(CSTA = $\overline{CSEL}$)[4]											
V_{OL}	I_{OL} = 1mA, V_{SC} = 0V			0.4			*			*	V
V_{OH}	V_{pullup} = 15V, V_{SC} = 0V	2.0	15		*	*		*	*		V

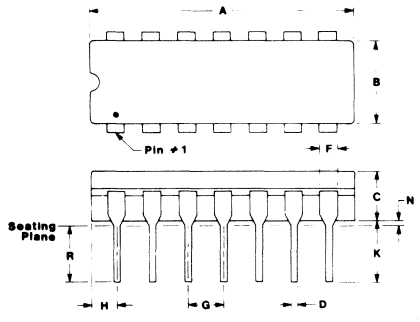
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	OPA201AG/RG			OPA201BG/SG			OPA201CG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL SIGNALS											
I_{OH} (OFF)			<1	20		•	•		•	•	µA
Switching Time											
Between Channels	$T_{MIN} \leq T_A \leq T_{MAX}$		5			•			•		µsec
CROSSTALK											
DC	V_{IN} to OFF	−100	−130		−120	•		−120	•		dB
60Hz	Channel = ±12V		−108			•			•		dB
TEMPERATURE RANGE (ambient)											
Specification											
A, B, C Grades		−25		+85	•		•	•		•	°C
S Grade					−55		+125				°C
Operating		−55		+125	•		•	•		•	°C
Storage		−65		+150	•		•	•		•	°C

NOTES:
1. 100% tested guaranteed fully warmed-up.
2. Without external adjustment. See Offset Adjustment section.
3. Over temperature specifications are $-55°C < T_A \leq +125°C$ for the S grade and $-25°C \leq T_A \leq +85°C$ for A, B, and C grades.
4. V_{TC} = Voltage on threshold control, pin 10. V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, I_{IL}, I_{OH}, I_{OL}, refers to voltage and current, input and output, high and low logic states.
5. Maximum voltage at Status Common must not be more positive than the Channel Select voltage (pin 11) or Threshold Control voltage (pin 10).

MECHANICAL

NOTES: 1. Leads in true position within 0.01" (0.25mm) R at seating plane.



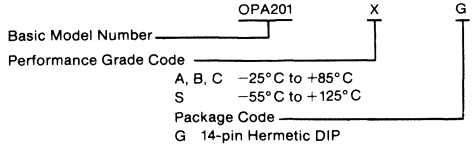
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.753	.767	19.13	19.48
B	.245	.251	6.22	6.38
C	.140	.170	3.56	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	—	.085	—	2.16
J	.008	.012	0.20	0.30
K	.150	—	3.80	—
L	0.3 BASIC		7.62 BASIC	
M	0°	15°	0°	15°
N	.009	.060	0.23	1.52
R	.125	.175	3.18	4.45

ABSOLUTE MAXIMUM RATINGS

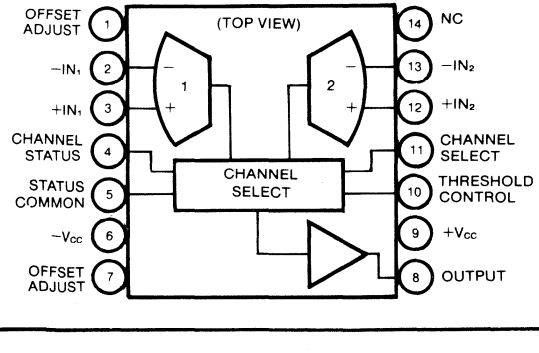
Supply	±18VDC
Internal Power Dissipation[1]	500mW
Differential Input Voltage[2]	±36VDC
Input Voltage Range[2]	±18VDC
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration[3]	Continuous
Junction Temperature	+175°C

NOTES:
1. $\theta_{JA} = 100°C/W$
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common or $\pm V_{CC}$.

ORDERING INFORMATION



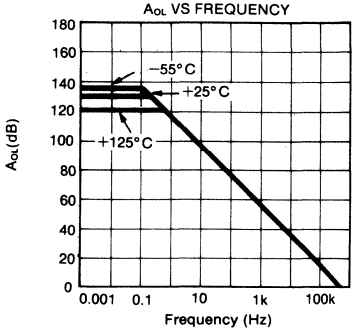
PIN CONFIGURATION



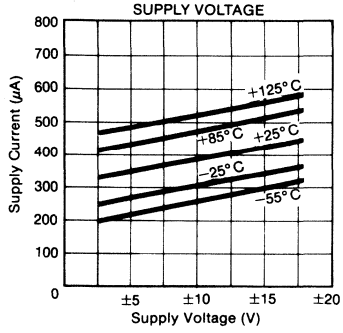
TYPICAL PERFORMANCE CURVES

(T_A = +25°C, ±V_{CC} = 15VDC, specifications are for either channel 1 or 2 unless otherwise noted.

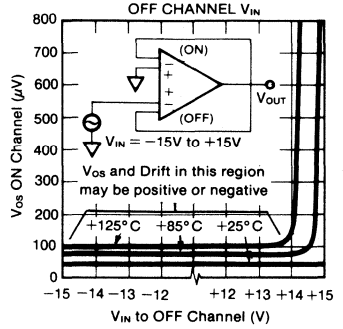
A_{OL} VS FREQUENCY



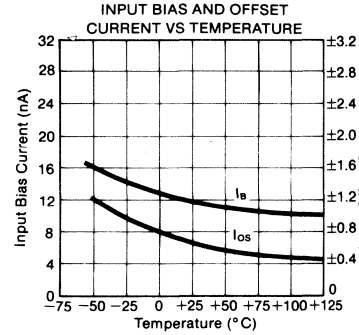
SUPPLY CURRENT VS SUPPLY VOLTAGE



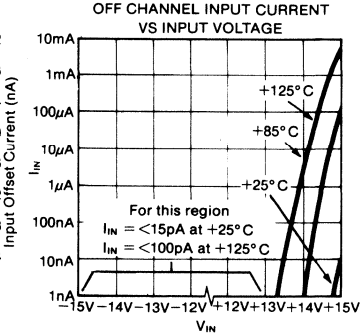
ON CHANNEL V_{OS} VS OFF CHANNEL V_{IN}



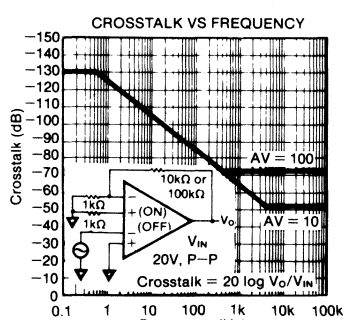
INPUT BIAS AND OFFSET CURRENT VS TEMPERATURE



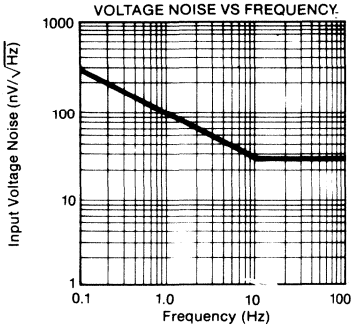
OFF CHANNEL INPUT CURRENT VS INPUT VOLTAGE



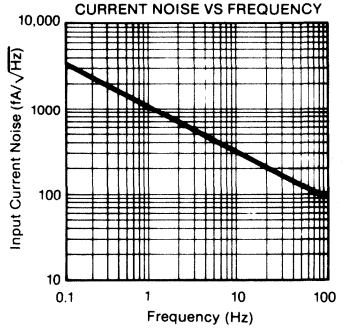
CROSSTALK VS FREQUENCY



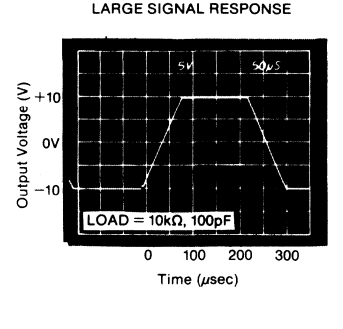
VOLTAGE NOISE VS FREQUENCY



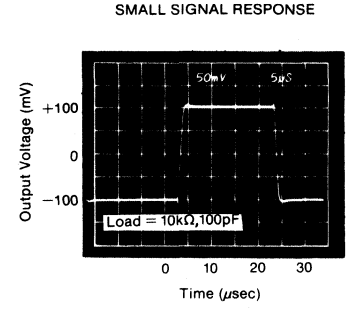
CURRENT NOISE VS FREQUENCY



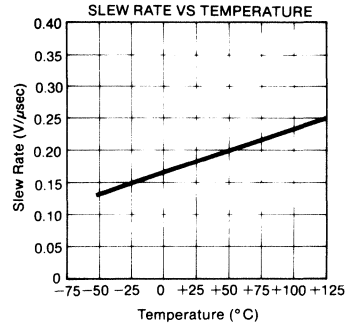
LARGE SIGNAL RESPONSE



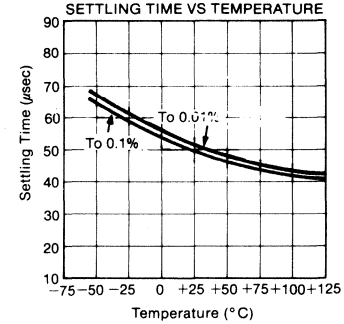
SMALL SIGNAL RESPONSE



SLEW RATE VS TEMPERATURE



SETTLING TIME VS TEMPERATURE



THEORY OF OPERATION

A simplfied schematic of the OPA201 Swop Amp is shown in Figure 1. The circuit has four main parts: (A) input stage 1, (B) input stage 2, (C) active load and output amplifier, and (D) channel select circuit. The two precision differential input stages are identical, with offset and drift laser-trimmed for very-tight matching. The input stages share a balanced, high precision active load and external offset adjust pins, so offset trim affects both channels (see "Using the Swop Amp" section for independent trim techniques). The input stages also share a gain stage and complementary output stage. The biasing circuits for the two input stages are well matched, so the characteristics of the two amplifiers are very nearly identical.

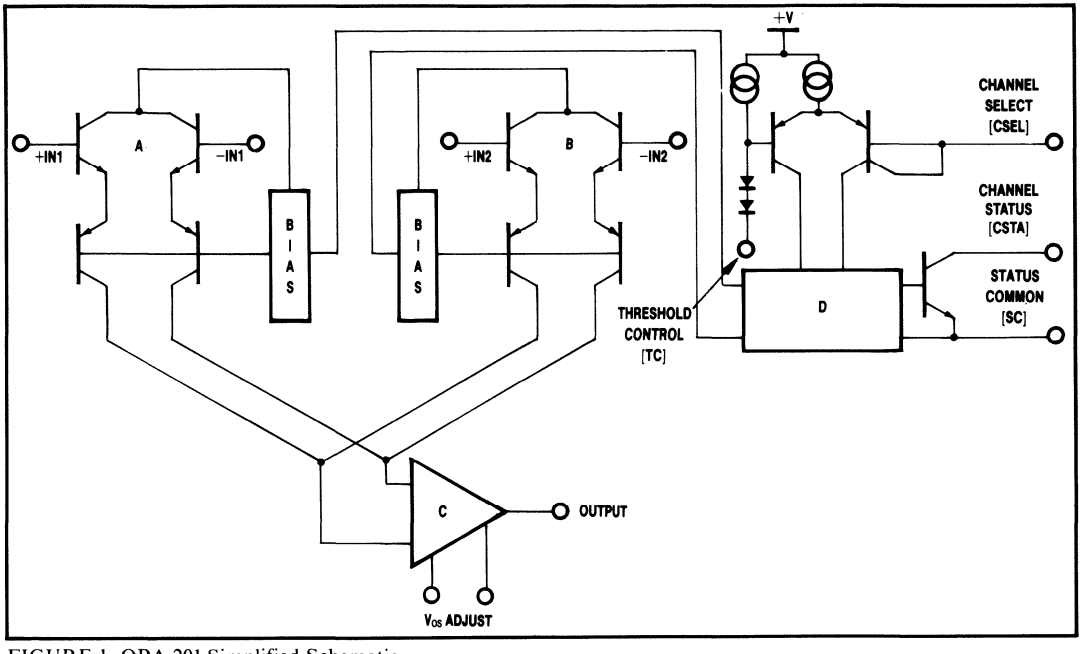


FIGURE 1. OPA 201 Simplified Schematic.

Under control of the channel select circuitry, only one input stage at a time is active. The selected input stage controls the output amplifier, while the unselected input stage is turned off by deactivating its bias circuitry. With no current in the unselected stage, it has negligible input bias current, and the OFF channel cannot send signals to the output amplifier (see Crosstalk specifications and Typical Performance Curves).

The channel select circuitry is simple but versatile, and its use is fully described in the "Using the Swop Amp" section. The trip point for changing channels is set by the threshold control, pin 10. This provides TTL-compatible levels for the channel select voltage on pin 11 when pin 10 is grounded. An open collector output transistor provides the logic inverse of the channel select voltage at the channel status pin. The emitter of this transistor, status common, is also brought out to a pin so the channel status can be referenced to ground or −V.

The complete circuit functions as a high precision operational amplifier which can switch between two sets of inputs under control of a 1-bit logic signal.

USING THE SWOP AMP

Designing with the Swop Amp is basically the same as designing with any precision operational amplifer, with the added versatility of switchable inputs. Feedback is connected from the output to each differential input to configure each channel as an inverting or noninverting amplifier, integrator, or other analog circuit function. The transfer functions for channels 1 and 2 may be identical to the point of sharing feedback elements, or they may be completely independent. Feedback resistors for the off channel are driven by the output as part of the load resistance. Error analysis involving E_{os}, I_B, I_{os}, and V_{cm} is the same as for any operational amplifier.

The OFF channel may be modeled as an open circuit in most applications, with input currents typically under 15pA for input voltages within the specified common-mode range (see Typical Performance Curves). Although crosstalk is specified for OFF channel input voltages equal to the common-mode input range extremes, the same crosstalk characteristics are typically observed for all input voltages between $-V_{CC}$ and $(+V_{CC} - 1VDC)$. Rejection of signals applied to the OFF channel's inputs is outstanding, as shown by the −120dB Crosstalk specifications and Typical Performance Curves for crosstalk versus frequency.

CHANNEL SELECTION

Four pins are involved in the channel select logic,

providing programmable input logic levels for channel select and an output status indicating which channel has been selected. Programmable logic levels allow the logic to be referenced to ground or virtually any voltage. Referencing the logic to −V is especially useful in applications where the supply voltage is low, for example ±3V. The pin-by-pin description and recommended connections describe the versatile but simple channel select techniques (refer to Figures 2 and 3).

Pin 10 - Threshold Control

Pin 10 sets the threshold voltage for channel switching, such that the switching point is two diode drops (≈1.3V) more positive than the Threshold Control voltage. This results in TTL compatibility when pin 10 is grounded. Pin 10 must be at least 5V more negative than $+V_{CC}$, and should be tied to $-V_{CC}$ when the minimum supply voltages are used (±2.5V or +5V). This results in TTL compatibility for logic referenced to $-V_{CC}$.

Pin 11 - Channel Select

The voltage on pin 11 determines which input stage is active. A logic high selects channel 1, logic low selects channel 2. Logic voltages are referenced to the Threshold Control, pin 10, and are TTL-, CMOS-, and open collector-compatible.

Pin 4 - Channel Status

Channel Status is an open collector output indicating which channel has been selected. It is the logic inverse of the Channel Select input referenced to Status Common, pin 5. This function is not required in many applications, and pin 4 should be left unconnected if not used. When using Channel Status, a pullup resistor is connected between pin 4 and a potential more positive than pin 5 (usually +V or ground). The logic low (indicating channel 1 selected) will be less than 0.4V more positive than pin 5 if the pullup resistor sets a current of 1mA or less. Logic high will be the voltage connected to the pullup resistor.

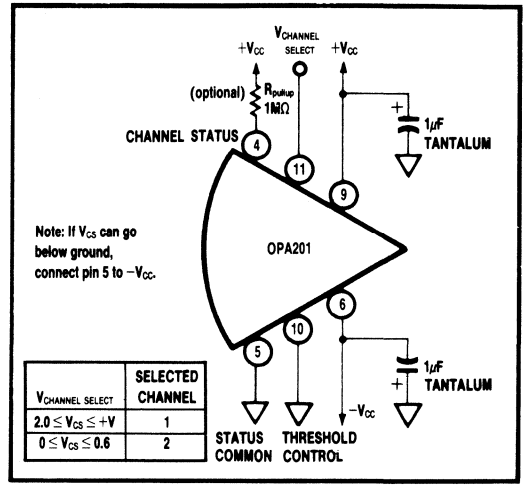
Pin 5 - Status Common

Status Common sets the reference point for Channel Status, and is usually connected to the same potential as the Threshold Control. Pin 5 must be more negative than pins 10 and 11 at all times, and should be connected to $-V_{CC}$ if the Channel Status function is not used. Status Common must be at least 5V more negative than $+V_{CC}$.

OFFSET ADJUSTMENT

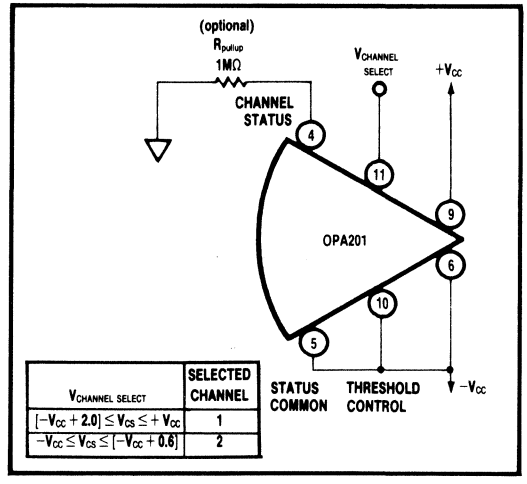
The input offset voltage is laser-trimmed and will not require user-adjustment for most applications. Pins 1 and 7 may be used to adjust the offset of the active channel to zero (see Figure 4). This will also affect the offset of the inactive channel (both offsets move in the same direction as the pot is adjusted). This technique may be used to make the offset for each channel equal in magnitude and opposite in polarity, which is desirable in many applications. Besides the complementary nature of the adjusted offsets, their magnitudes will now be less than one-half of the V_{os} match specification.

An inexpensive CMOS IC, CD4007 (dual-Complementary Pair Plus Inverter), may be used to alternately connect dual-offset adjust potentiometers (see Figure 5) allowing independent V_{os} adjustment. In this circuit, the channel status output from the Swop Amp is used to drive the CMOS logic, which connects one wiper or the



VCHANNEL SELECT	SELECTED CHANNEL
2.0 ≤ VCS ≤ +V	1
0 ≤ VCS ≤ 0.6	2

FIGURE 2. Channel Selection for Ground-Referenced Channel Select Signals.



VCHANNEL SELECT	SELECTED CHANNEL
[−VCC + 2.0] ≤ VCS ≤ +VCC	1
−VCC ≤ VCS ≤ [−VCC + 0.6]	2

FIGURE 3. Channel Selection for $-V_{CC}$ Referenced Logic Signals.

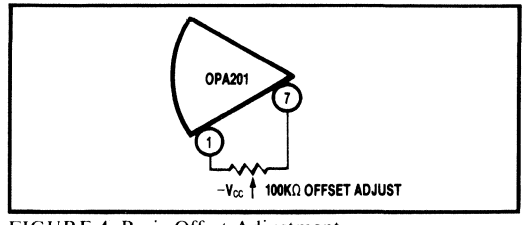


FIGURE 4. Basic Offset Adjustment.

other to $-V_{CC}$. Thus R_1 adjusts the offset of channel 1 while R_2 affects the offset only when channel 2 is selected.

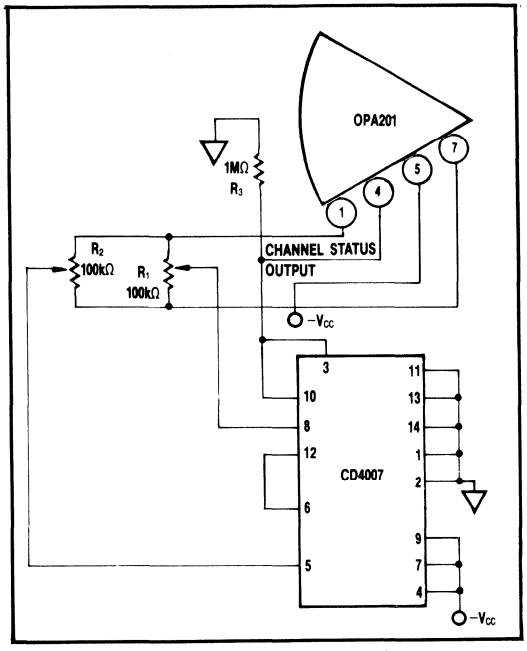


FIGURE 5. Independent Dual-Offset Adjustment.

Note: The CMOS logic requires $-V_{CC}$ (3V minimum) and common. The Status Common (pin 5) must be connected to $-V_{CC}$.

APPLICATIONS

The OPA201 is ideal for a variety of applications where a precision amplifier and switch are needed. Since the two input stages are contained on the same IC and are precision laser-trimmed, their offsets match very closely. Therefore, the OPA201 can be used as an auto-zeroing circuit as well as a dual-channel or switchable-gain amplifier. It can also be extended to become a low power 4-channel Swop Amp or dual-channel instrumentation amplifier under control of TTL level logic. General purpose and unique applications are only limited by the user's imagination.

Software auto-zeroing using the Swop Amp is easy to perform (Figure 6). One channel processes signals and the other channel has the input grounded (both channels have the same gain). The system generating the error signal may be a VFC, Iso Amp, ADC, Modulator, etc. When the zero-input channel is selected,

$$V_{out} = V_{error} + A_V V_{os2}$$

V_{error} = system error voltage
V_{os2} = Channel 2 V_{os}
A_V = Swop Amp voltage gain $= 1 + (R_2/R_1)$

When the signal channel is selected,

$$V_{out} = V_{error} + A_V V_{os1} + A_V V_{IN}$$

Subtracting the "zero" V_o from signal V_o leaves a corrected output voltage

$$V_{0ut} = A_V V_{IN} + A_V (V_{os1} - V_{os2})$$
$$= A_V (V_{IN} + \Delta V_{os})$$

Using this technique, system errors may be reduced to the V_{os} match error (50μV for CG grade) of the Swop Amp. Obviously the channel used for zeroing could have a voltage reference or AC waveform for gain calibration for an input, instead of ground.

Auto-zeroing may be free-running, with the Swop Amp functioning as a chopper, by connecting an oscillator to the channel select. Figure 6 shows pin 10 grounded, which allows TTL level interfacing. By programming this pin with a voltage level, other logic levels can be accommodated.

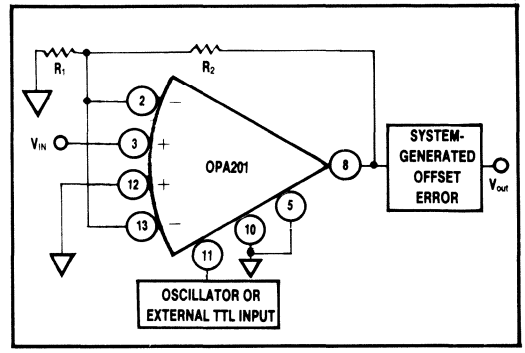


FIGURE 6. Input Amplifier for Auto-Zeroing Systems.

The OPA201 requires only external resistors to make a dual-channel amplifier (2-channel multiplexer with gain). Gain for either channel may be noninverting (Figure 7) or inverting (Figure 8) with the usual operational amplifier gain equations applying in each case. In the noninverting case, feedback is connected from the output to each input, with a common feedback resistor for equal gains. The advantage, in inverting gain circuits, is that the signal does not produce a common-mode voltage which can introduce error or input swing limitations. This is especially important in low supply voltage applications where common-mode range becomes limited. Also one channel can be noninverting and the other inverting, which is particularly useful in absolute value circuits. Note that in order to achieve the specified open-loop gain and maximum output voltage swing, the total output load including both feedback networks should not exceed 10kΩ (see Figures 7 and 8).

Amplifiers with switchable transfer functions are designed much like dual-channel amplifiers, except both inputs are connected in parallel, with each channel configured for a different transfer function. Figure 9 shows a circuit that has a gain of 10 for Channel Select HIGH (channel 1 selected) and a gain of 1000 for Channel Select LOW (channel 2 selected). In this case, the channel select may be thought of as a gain select.

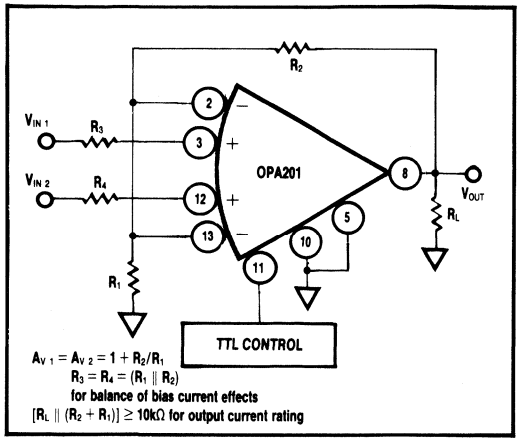


FIGURE 7. Selectable Input Amplifier, Noninverting.

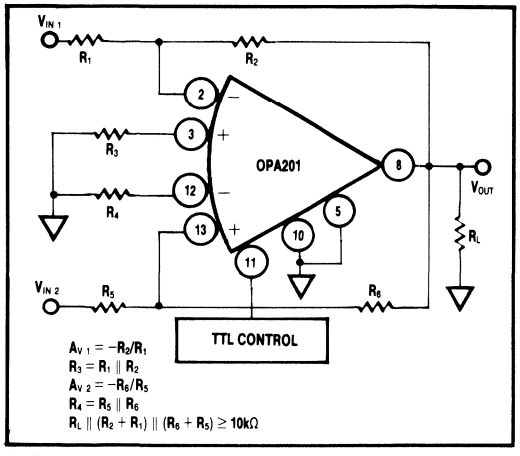


FIGURE 8. Selectable Input Amplifier, Inverting.

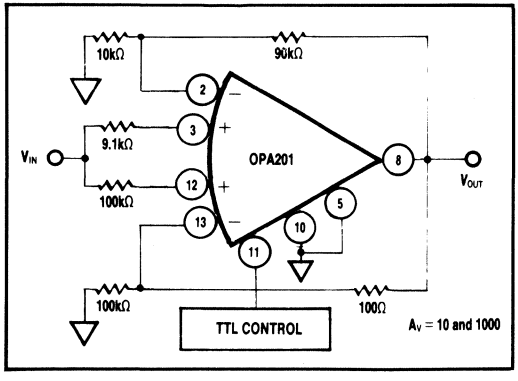


FIGURE 9. Switchable Gain Amplifier.

This concept also applies to switchable bandwidth circuits, where AC coupling (high-pass) or smoothing (low-pass) characteristics need to be switched in under digital control. A wide variety of operational amplifier function circuits may be made selectable or switchable using these techniques.

Figure 10 shows a two-channel differential amplifier. This concept can be expanded to a full high input impedance instrumentation amplifier by adding four input buffer amplifiers or by using two front end Swop Amps followed by an operational amp (Figure 11).

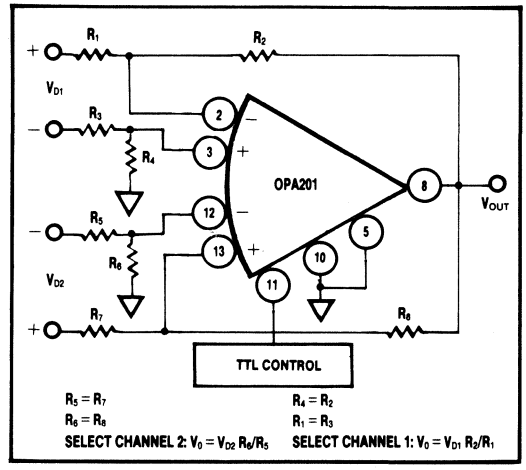


FIGURE 10.Low Power Dual-Channel Differential Amplifier.

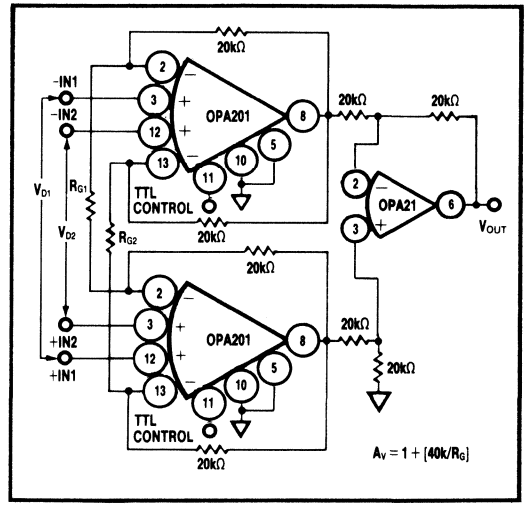
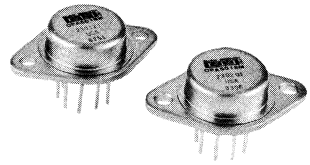


FIGURE 11. Low Power Dual-Channel Instrumentation Amplifier.

BURR-BROWN®



OPA501

High Current - High Power OPERATIONAL AMPLIFIER

FEATURES

- WIDE SUPPLY RANGE
  ±10 to ±40 Volts
- HIGH OUTPUT CURRENT
  ±10 Amps Peak
- HIGH OUTPUT POWER
  260 Watts Peak
- SMALL SIZE: TO-3 PACKAGE

APPLICATIONS

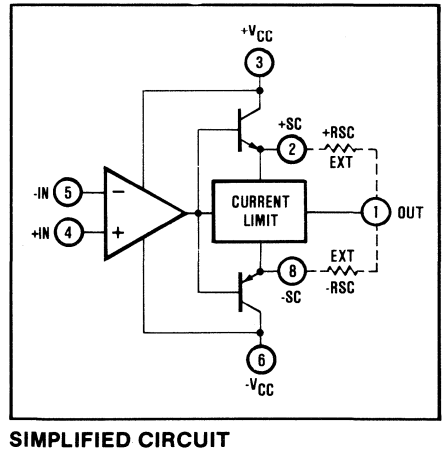
- SERVO AMPLIFIER
- MOTOR DRIVER
- ACTUATOR CONTROL
- AUDIO AMPLIFIER
- SYNCRO DRIVER
- POWER SUPPLY REGULATOR

DESCRIPTION

The OPA501 is a high power operational amplifier. Its high current output stage delivers ±10A yet the amplifier is unity-gain stable and it can be used in any operational amplifier configuration. The 260W peak output capability allows the OPA501 to drive loads (such as motors) with a greater safety margin.

Safe operating area is fully specified and output current limiting is provided to protect both the amplifier and the load from excessive current.

This hybrid IC is housed in an 8-pin hermetic TO-3 package. The electrically-isolated package allows direct mounting to chassis or heat sink without an insulating washer or spacer which would increase thermal resistance.



SIMPLIFIED CIRCUIT

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C and $\pm V_{CC}$ = 28VDC (OPA501RM/AM); $\pm V_{CC}$ = 34VDC (OPA501SM/BM) unless otherwise noted.

PARAMETER	CONDITIONS	OPA501RM/AM MIN	OPA501RM/AM TYP	OPA501RM/AM MAX	OPA501SM/BM MIN	OPA501SM/BM TYP	OPA501SM/BM MAX	UNITS
RATED OUTPUT(1)(2)								
Output Current,	R_L = 2Ω (RM/AM)	±10			*			A
Continuous(3)	R_L = 2.6Ω (SM/BM)	±10			*			A
Output Voltage(3)	I_O = 10A peak	±20	23		±26	±29		V
DYNAMIC RESPONSE								
Bandwidth, Unity Gain	Small Signal		1			*		MHz
Full Power Bandwidth	V_O = 40Vp-p, R_L = 8Ω	10	16		*	*		kHz
Slew Rate	R_L = 5Ω (RM/AM)	1.5			*			V/µsec
	R_L = 6.5Ω (SM/BM)	1.5			*			V/µsec
INPUT OFFSET VOLTAGE								
Initial Offset			±5	±10		±2	±5	mV
vs Temperature	-25°C < T < +85°C (RM/AM)		±10	±65				µV/°C
	-55°C < T < +125°C (SM/BM)					±10	±40	µV/°C
vs Supply Voltage			±35			*		µV/V
INPUT BIAS CURRENT								
Initial	T_{case} = +25°C		15	40		*	20	nA
vs Temperature			±0.05			*		nA/°C
vs Supply Voltage			±0.02			*		nA/V
INPUT DIFFERENCE CURRENT								
Initial	T_{case} = +25°C		±5	±10		±2	±3	nA
vs Temperature	-25°C < T < +85°C (RM/AM)		±0.01					nA/°C
	-55°C < T < +125°C (SM/BM)					±0.01		nA/°C
OPEN-LOOP GAIN, DC	R_L = 5Ω (RM/AM)	94	115					dB
	R_L = 6.5Ω (SM/BM)				98	115		dB
INPUT IMPEDANCE								
Differential			10			*		MΩ
Common-mode			250			*		MΩ
INPUT NOISE								
Voltage Noise	f_n = 0.3Hz to 10Hz		3			*		µV, p-p
	f_n = 10Hz to 10kHz		5			*		µV, rms
Current Noise	f_n = 0.3Hz to 10Hz		20			*		pA, p-p
	f_n = 10Hz to 10kHz		4.5			*		pA, rms
INPUT VOLTAGE RANGE								
Common-mode Voltage(4)	Linear Operation	±(|V_{CC}|-6)	±(|V_{CC}|-3)		*	*		V
Common-mode Rejection	F = DC, V_{CM} = ±(|V_{CC}|-6)	70	110		80	*		dB
POWER SUPPLY								
Rated Voltage			±28			±34		V
Operating Voltage Range		±10		±36	*		±40	V
Current, quiescent			±2.6	±10		*	*	mA
TEMPERATURE RANGE	case							
Specification, RM/SM		-55		+125	*		*	°C
AM/BM		-25		+85	*		*	°C
Operating, derated performance, AM/BM		-55		+125	*		*	°C
Storage		-65		+150	*		*	°C
THERMAL RESISTANCE	Steady State θ_{JC}		2.0	2.2		*	*	°C/W

*Specification same as for OPA501RM/AM.

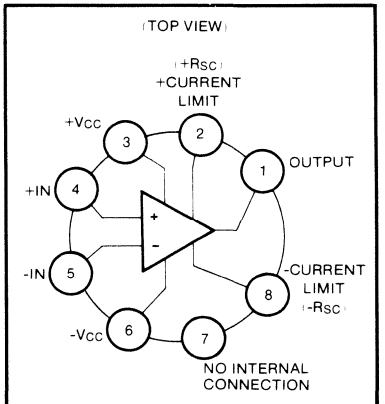
NOTES:
1. Package must be derated based on a junction to case thermal resistance of 2.2° C/W or a junction to ambient thermal resistance of 30° C/W.
2. Safe Operating Area and Power Derating Curves must be observed.
3. With $\pm R_{SC}$ = 0. Peak output current is typically greater than 10A if duty cycle and pulse width limitations are observed. Output current greater than 10A is not guaranteed.
4. The absolute maximum voltage is 3V less than supply voltage.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage (V_{CC})	±40VDC
Power dissipation at +25°C[1][2]	79W
Differential input voltage	$\pm V_{CC}$-3V
Common-mode input voltage	$\pm V_{CC}$
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10sec)	+300°C
Junction temperature	+200°C
Output short-circuit duration[3]	continuous

NOTES:
1. At case temperature of +25° C. Derate at 2.2° C/W above case temperature of +25° C.
2. Average dissipation.
3. Within safe operating area and with appropriate derating.

CONNECTION DIAGRAM

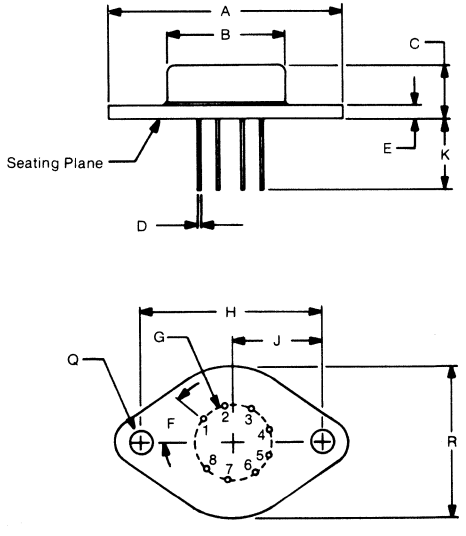


ORDERING INFORMATION

OPA501 X M

Basic Model Number	
Performance Grade Code	
A, B = -25° C to +85° C	OPA501AM
	OPA501BM
R, S = -55° C to +125° C	OPA501RM
	OPA501SM
Package Code	
TO-3	OPA501SM/883

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.

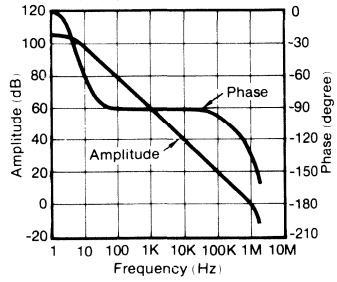
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.510	1.550	38.35	39.37
B	.745	.770	18.92	19.56
C	.300	.400	7.62	10.16
D	.038	.042	0.97	1.07
E	.080	.105	2.03	2.67
F	40° BASIC		40° BASIC	
G	.500 BASIC		12.7 BASIC	
H	1.186 BASIC		30.12 BASIC	
J	.593 BASIC		15.06 BASIC	
K	.400	.500	10.16	12.70
Q	.151	.161	3.84	4.09
R	.980	1.020	24.89	25.91

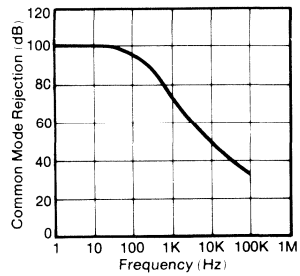
TYPICAL PERFORMANCE CURVES

(Typical at +25° case and ±V_{CC} = 28VDC unless otherwise noted.)

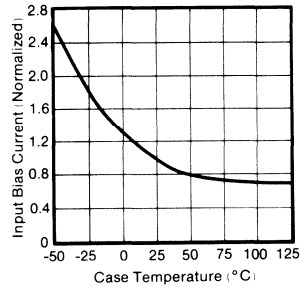
OPEN-LOOP FREQUENCY RESPONSE



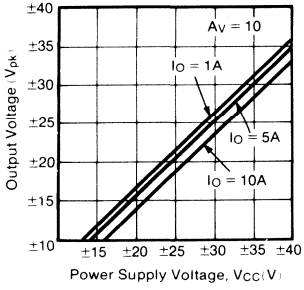
COMMON MODE REJECTION VS FREQUENCY



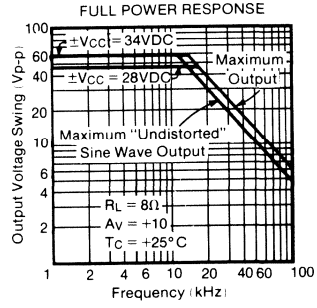
INPUT BIAS CURRENT VS TEMPERATURE



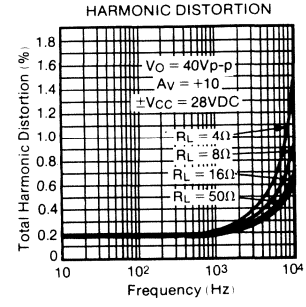
OUTPUT VOLTAGE SWING VS POWER SUPPLY VOLTAGE



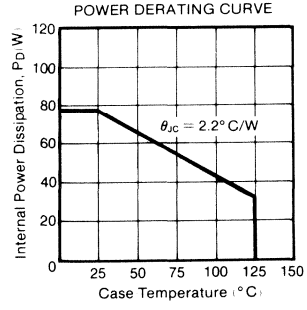
FULL POWER RESPONSE



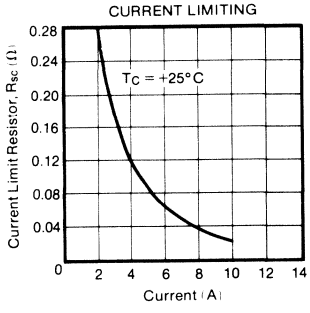
HARMONIC DISTORTION



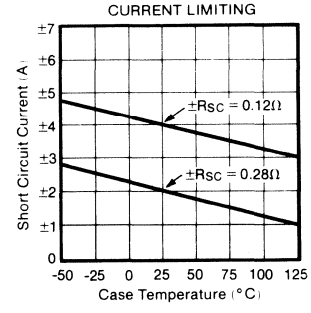
POWER DERATING CURVE



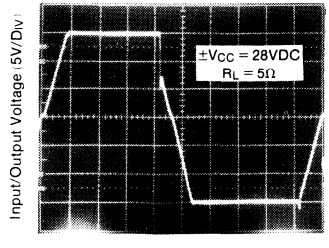
CURRENT LIMITING



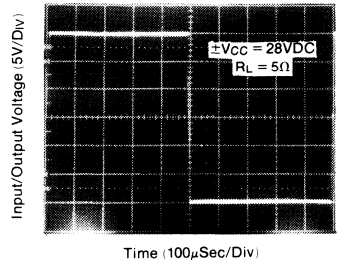
CURRENT LIMITING



PULSE RESPONSE, AV = +1



PULSE RESPONSE, AV = +1



INSTALLATION AND OPERATING INSTRUCTIONS

PROPER GROUNDING AND POWER SUPPLY BYPASSING

Particular attention should be given to proper grounding practices because the large output currents can cause significant ground-loop errors. Figure 1 illustrates proper connections.

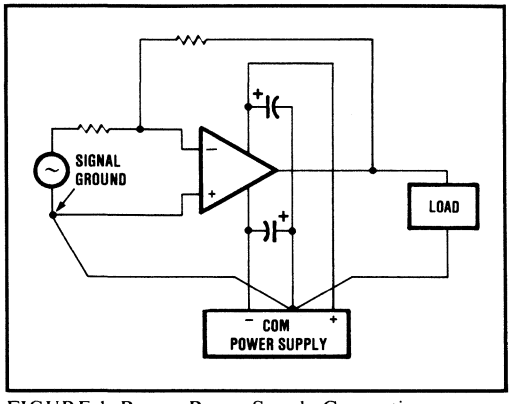


FIGURE 1. Proper Power Supply Connections.

Note that the connections are such that the load curent does not flow through the wire connecting the signal ground point to the power supply common. Also, power supply and load leads should be run physically separated from the amplifier input and signal leads.

The amplifier should be power-supply-bypassed with 50μF tantalum capacitors connected as close to pins 3 and 6 as possible. The capacitors should be connected to the load ground rather than the signal ground.

CURRENT LIMITS

The OPA501 amplifier is designed so that both the positive and negative load current limits can be set independently with external resistors R_{+SC} and R_{-SC} respectively. The approximate value of these resistors is given by the equation:

$$R_{SC} = \left(\frac{0.65}{I_{LIMIT}} - 0.0437\right) \text{ ohms}$$

I_{LIMIT} is the desired maximum current in amperes. The power dissipation of the current limit resistor is:

$$P_{max} = R_{SC} (I_{LIMIT})^2 \text{ watts}$$

R_{SC} is in ohms and I_{LIMIT} is in amperes.

Current limit resistors carry the full amplifier output current so lead lengths should be minimized. Highly inductive resistors can cause loop instability. Variation in I_{LIMIT} with case temperature is shown in the Typical Performance Curves.

The amplifier should be used with as low a current limit as possible for its particular application. This will minimize the chance of damaging the amplifier under abnormal load conditions and will increase reliability by limiting internal power dissipation.

The current limits may be used to generate other functions such as constant current supplies and torque or stall current limits for servomotor applications.

HEAT SINKING

The OPA501 requires a heat sink to limit output transistor junction temperature (T_J) to an absolute maximum of +200°C. The steady-state thermal circuit is illustrated in Figure 2.

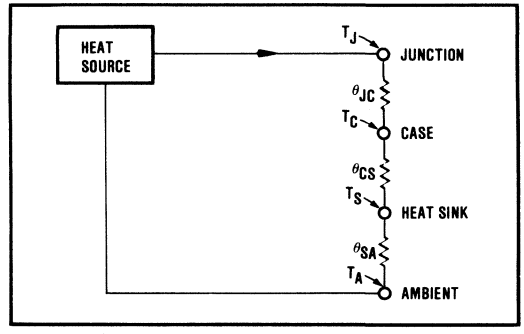


FIGURE 2. Simplified Steady-State Heat Flow Model.

Junction temperature (T_J) is found from the equation:

$$T_J = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$

Where P_D = average amplifier power dissipation (W)
θ_{JC} = junction to case thermal resistance (°C/W)
θ_{CS} = device mounting thermal resistance (°C/W)
θ_{SA} = heat sink thermal resistance (°C/W)
T_A = ambient temperature (°C)

For most heat sink calculations the quiescent power dissipation is very low (<1 watt) and can be disregarded with only a small error.

The minimum size heat sink can be found from the equation:

$$\theta_{SA} = \frac{T_J - T_A}{P_D} - \theta_{CS} - \theta_{JC}$$

Example: Find the maximum thermal resistance (smallest heat sink) that can be used for an OPA501 with $\pm V_{CC}$ = 28VDC. Output voltage is +10VDC across a 10Ω resistor and ambient temperature is +50°C:

$$P_D = [(+28\text{VDC}) - (+10\text{VDC})] \times \frac{+10\text{VDC}}{10\Omega} = 18\text{W}$$

$$\theta_{SA} = \frac{200°\text{C} - 50°\text{C}}{18\text{W}} - 0.1°\text{C/W} - 2.2°\text{C/W}$$

θ_{SA} = 6.03°C/W maximum

As large a heat sink as possible should be used. θ_{CS} depends on the flatness of the heat sink, the thermal compound used, and the roughness of the mating surfaces. Typical values are between 0.1°C/W and 0.3°C/W for a TO-3 package properly mounted on a heat sink.

The OPA501 mounting flange is electrically-isolated and can be mounted directly to a heat sink without insulating washers or spacers. Screws with Bellville spring washers are recommended to maintain positive clamping pressure on heat sink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase θ_{CS}.

The output transistor thermal resistance (θ_{JC}) is a function of output current pulse width, pulse shape, and duty cycle. Long duration pulses allow the junction temperature to approach its steady state value while shorter pulses cause a lower peak junction temperature due to the junction's thermal time constant. Heat is conducted rapidly away from the junction so that as duty cycle decreases, junction temperature decreases.

Steady state θ_{JC} is rated at 2.2°C/W maximum. In applications where the amplifier's output current alternates between output transistors–for example, an AC amplifier–the transistor θ_{JC} will depend on frequency as shown in Figure 3.

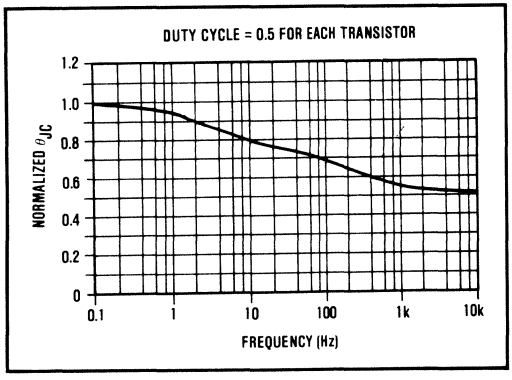


FIGURE 3. Effective θ_{JC} for Applications Where Output Current Alternates Between Output Transistors.

Example: OPA501SM with $\pm V_{CC}$ = 28VDC; heat sink θ_{SA} = 0.4°C/W; output = 11.2VAC, rms 400Hz at 5A, rms; Power Factor = 1.0; assume a mounting resistance of 0.1°C/W and an ambient temperature of +25°C.

Peak output voltage is: (11.2V, rms) $\sqrt{2}$ = 15.84V,pk

Peak voltage across each output transistor is:
28V - 15.84V = 12.16V, pk

Peak output current is: (5A, rms) $\sqrt{2}$ = 7.07A, pk

Peak power dissipated by each output transistor is:
(12.16V, pk) (7.07A, pk) (1.0) = 85.97W, pk

From Figure 3, the effective value of θ_{JC} is 0.60 × rated θ_{JC}, therefore,
θ_{JC} = 1.32°C/W for this example.

The peak junction temperature will be:
T_J = 85.97W (1.32°C/W + 0.1°C/W + 0.4°C/W) +25°C
T_J = 181.5°C/W

This is below the maximum junction temperature limits of +200°C, but a lower T_J will increase the amplifier's reliability. In this case, a lower $\pm V_{CC}$ could be used to reduce dissipation.

At lower frequencies, the junction temperature can show greater modulation as the output power transistor dissipation increases and decreases with output voltage and current swing. To ensure that the maximum junction temperature is not exceeded, use the appropriate value of effective θ_{JC} from Figure 3.

To illustrate the importance of considering frequency, consider the previous example, but with the amplifier operating at 60Hz:

For a 60Hz output
the effective θ_{JC} = 0.72 × rated θ_{JC} = 1.58°C/W
T_J = 85.97W (1.58°C/W + 0.1°C/W + 0.4°C/W) + 25°C
T_J = 204°C: UNACCEPTABLE

NOTE: Maximum dissipation does not occur at maximum output.

SAFE OPERATING AREA (SOA)

In addition to the limits imposed by power dissipation, the amplifier's output transistors are also limited by a second breakdown region. This occurs because of increased emitter current density due to current crowding at higher operating voltages. Both the dissipation and second breakdown limits depend on time and temperature. Figure 4 shows each output transistor's SOA at a case temperature of +25°C.

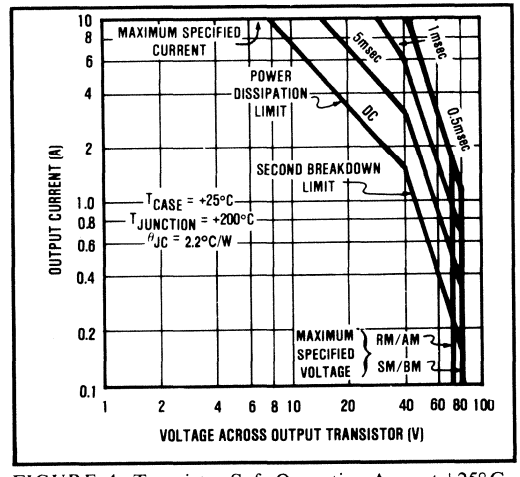


FIGURE 4. Transistor Safe Operating Area at +25°C Case Temperature.

Limits for short pulse widths are substantially greater than for steady state (DC). At a case temperature of +125°C the SOA limits are reduced (see Figure 5). The SOA shown in these curves is based on a conservative linear derating of both the power dissipation and the second breakdown region.

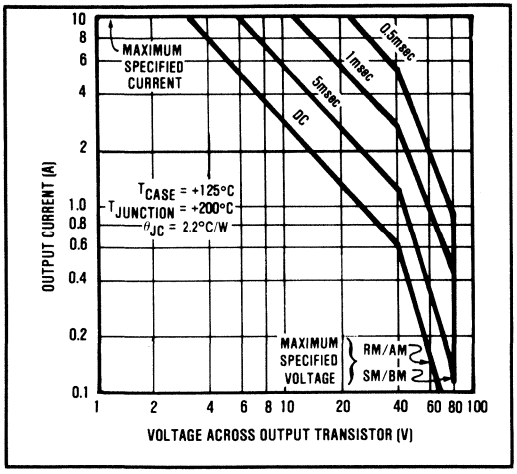


FIGURE 5. Transistor Safe Operating Area at +125°C Case Temperature.

Resistive loads are easy to analyze by simply plotting load lines on the SOA curve. If the curve representing the load line stays within the OPA501 output transistor SOA curve and all other parameters are observed, such as case temperature, etc., the amplifier will be safe. The load line can swing through the larger SOA limits if their time duration constraints are strictly observed.

Reactive loads present a more complex problem since the output voltage and current are not in phase. This results in the reactive load line becoming elliptical (when plotted on linear axes) which requires a larger SOA for safe operation.

Although detailed analysis is beyond the scope of this data sheet, the load line can be viewed on an oscilloscope as shown in Figure 6. The X-Y display is driven by the voltage across the load and by the current into the load.

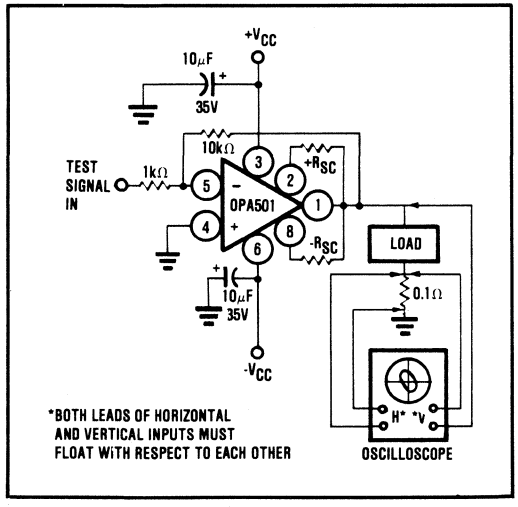


FIGURE 6. Loadline Display.

This set up can also display voltage and current stress across the OPA501 output transistors as shown in Figure 7. This data can then be compared to the SOA limits.

The amplifier is designed to operate with electromotive-force-generating loads such as servomotors, relays, and actuators. Careful attention must be paid to both the load characteristics and the amplifier's SOA to ensure safe operation.

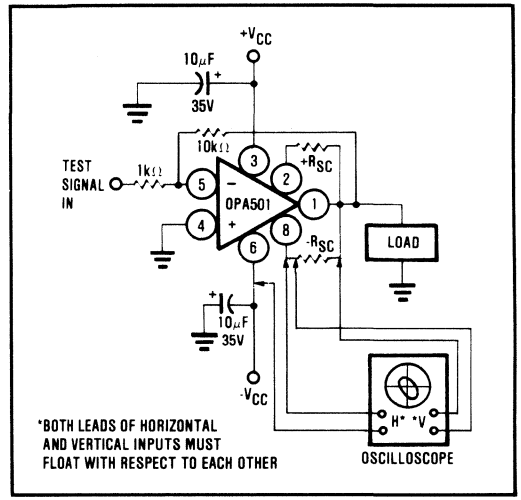


FIGURE 7. Output Transistor Safe Operating Area Stress Display.

Figure 8 shows the OPA501 configured as a DC permanent magnet motor driver. The armature current (I_A) and motor voltage (V_m) are monitored within an oscilloscope in the X-Y mode displaying I_A and V_m respectively. Slewing the motor with a 4Hz sine wave results in the motor power ellipse of Figure 9. The input level has been adjusted to give ±20V, pk, across the motor. An examination of the power ellipse indicates that the instan-

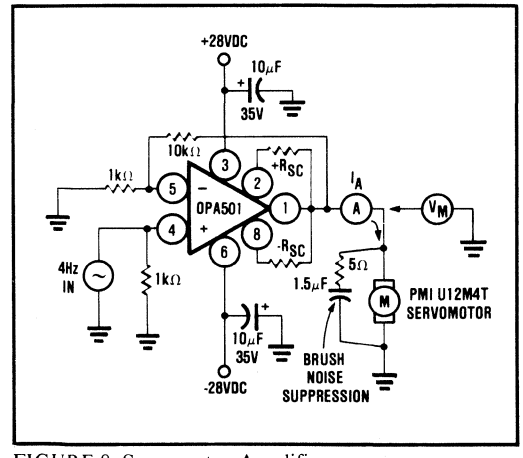


FIGURE 8. Servomotor Amplifier.

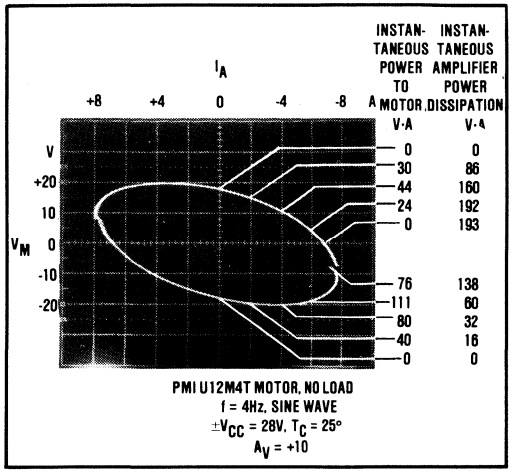


FIGURE 9. D.C. Servomotor Load Line.

taneous power delivered to the motor exceeds the amplifier output transistor's safe operating area at a case temperature of +25°C. The point at which the motor shows 0V at -6.9A is a problem. The voltage across the output transistor is 28V - 0V = 28V. Checking the SOA curve shows that the amplifier can safely withstand this condition for slightly under 5msec. At 4Hz this transient swing outside the DC SOA region is exceeded for much longer than 5msec. Continued operation under these conditions will result in failure. Peak junction temperatures should not exceed +200°C. Perhaps a motor with a higher impedance winding should be considered for this application. Current limiting and lower supply voltage can also reduce dissipation.

Motors used in servo applications often required a surprisingly large current to accelerate quickly. Worst case conditions occur when the motor is operating at full speed and is suddenly slammed into reverse ("plugging"). This condition is illustrated in Figure 10 when a DC servomotor is driven by a bipolar square wave. As the motor reverses direction a large surge current flows, causing very high peak power dissipation in the amplifier. After several time constants (determined by the inertia moment) the current drops to a lower steady-state value. Loading the motor increases the motor average power and amplifier dissipation. SOA curves should be checked for safe operation under these surge conditions.

The OPA501 current limits may be set to clip the high surge currents to a safe level. This is shown in Figure 11. Note that the current limit does limit the servo motor peak acceleration.

Inductive loads should be investigated for high peak transients generated by a collapsing magnetic field. Resistive damping can reduce this problem and although the amplifier has substrate diodes as part of the Darlington output transistor structure, external diodes are recommended for heavy clamping.

Fast diodes such as those normally used as rectifiers in switching power supplies are suitable.

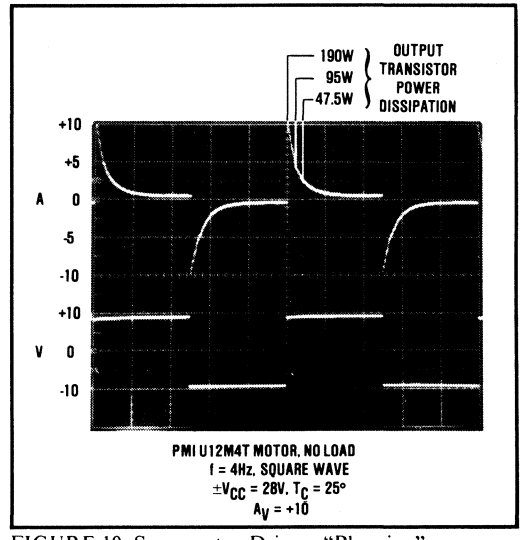


FIGURE 10. Servomotor Drive – "Plugging"

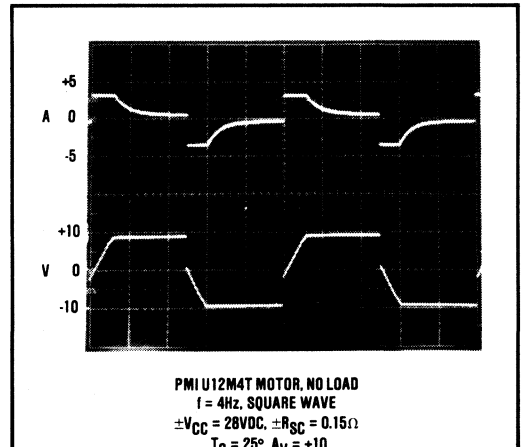


FIGURE 11. Servomotor Drive With Current Limit.

BURR-BROWN®

INA104

Very-High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- VERSATILE FOUR-OP AMP DESIGN
- ULTRA-LOW VOLTAGE DRIFT - 0.25μV/°C, max
- LOW OFFSET VOLTAGE - 25μV, max
- LOW NONLINEARITY - 0.002%, max
- LOW NOISE - 13nV/$\sqrt{Hz}$ at f_0 = 1kHz
- HIGH CMR - 106dB at 60Hz, min
- HIGH INPUT IMPEDANCE - $10^{10}\Omega$
- LOW COST

APPLICATIONS

- AMPLIFICATION OF SIGNALS FROM SOURCES SUCH AS:
  - Strain Gages
  - Thermocouples
  - RTDs
- REMOTE TRANSDUCER AMPLIFIER
- LOW LEVEL SIGNAL CONDITIONER
- MEDICAL INSTRUMENTATION

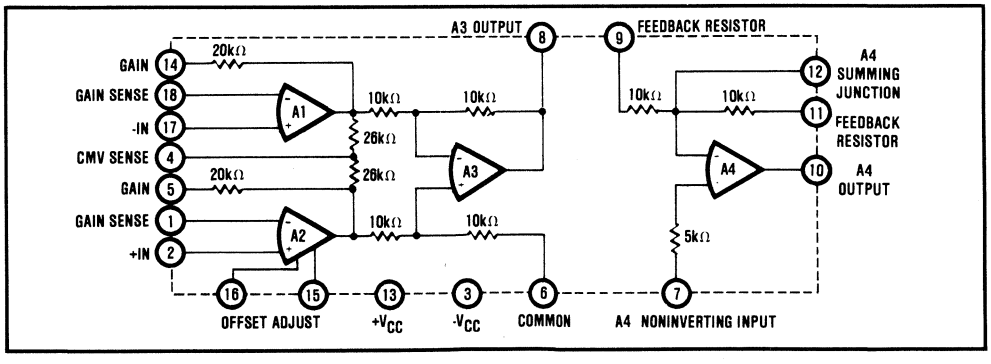
DESCRIPTION

The INA104 is a high accuracy, multistage, integrated-circuit instrumentation amplifier designed for signal conditioning requirements where very-high performance is desired.

A multiamplifier, monolithic design, which uses Burr-Brown's ultra-low drift, low noise technology, provides the highest performance with maximum versatility at the lowest cost and this makes the INA104 ideal for even high volume applications.

Burr-Brown's compatible thin-film resistors and state-of-the-art wafer level laser-trimming techniques are used for minimizing offset voltage and temperature drift. This advanced technique also maximized common-mode rejection and gain accuracy.

The INA104 also contains a fourth operational amplifier, specified separately, which can conveniently be used for some important applications such as single capacitor active low-pass filtering, easy output level shifting, Common-mode voltage active guard drive, and increased gain (x 10,000 and greater).



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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C with ±15VDC power supply and in circuit of Figure 1 unless otherwise noted.

	INA104HP			INA104JP			INA104KP			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INSTRUMENTATION AMPLIFIER										
GAIN										
Range of Gain	1		1000	*		*	*		*	V/V
Gain Equation		G = 1 + (40k/R_G)			*			*		V/V
Error From Equation, DC(1)		±(0.08 - 0.05/G)	±(0.15 - 0.1/G)		*	*		*	*	% of FS
Gain Temp. Coefficient(2)										
G = 1		2	5		*	*		*	*	ppm/°C
G = 10		20	50		*	*		*	*	ppm/°C
G = 100		22	55		*	*		*	*	ppm/°C
G = 1000		22	55		*	*		*	*	ppm/°C
Nonlinearity, DC		±(0.002 + 10^{-5}G)	±(0.005 + 2 x 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)		±(0.001 + 10^{-5}G)	±(0.002 + 10^{-5}G)	% of p-p FS
RATED OUTPUT										
Voltage	±10	±12.5		*	*		*	*		V
Current	±5	±12.5		*	*		*	*		mA
Output Impedance		0.2			*			*		Ω
INPUT OFFSET VOLTAGE										
Initial Offset at +25°C(3)		±25 ±200/G	±50 ±400/G		±10 ±100/G	±25 ±200/G		±10 ±100/G	±25 ±200/G	µV
vs Temperature			±2 ±20/G			±0.75 ±10/G			±0.25 ±10/G	µV/°C
vs Supply		±(1 + 50/G)			*			*		µV/V
vs Time		±(1 + 20/G)			*			*		µV/mo
INPUT BIAS CURRENT										
Initial Bias Current (each input)		±15	±30		±10	*		±5	±20	nA
vs Temperature		±0.2			*			*		nA/°C
vs Supply		±0.1			*			*		nA/V
Initial Offset Current		±5	±30		±2	*		±2	±20	nA
vs Temperature		±0.5			*			*		nA/°C
INPUT IMPEDANCE										
Differential		10^{10} || 3			*			*		Ω || pF
Common-mode		10^{10} || 3			*			*		Ω || pF
INPUT VOLTAGE RANGE										
Range, Linear Response	±10			*			*			V
CMR with 1kΩ Source Imbal.										
DC to 60Hz, G = 1	80	90		*	*		*	*		dB
DC to 60Hz, G = 10	96	106		*	*		*	*		dB
DC to 60Hz, G = 100 to 1000	106	110		*	*		*	*		dB
INPUT NOISE										
Input Voltage Noise										
f_B = 0.01Hz to 10Hz		0.8			*			*		µV, p-p
Density, G = 1000										
f_o = 10Hz		18			*			*		nV/√Hz
f_o = 100Hz		15			*			*		nV/√Hz
f_o = 1kHz		13			*			*		nV/√Hz
Input Current Noise										
f_B = 0.01Hz to 10Hz		50			*			*		pA, p-p
Density										
f_o = 10Hz		0.8			*			*		pA/√Hz
f_o = 100Hz		0.46			*			*		pA/√Hz
f_o = 1kHz		0.35			*			*		pA/√Hz
DYNAMIC RESPONSE										
Small Signal, ±3dB Flatness										
G = 1		300			*			*		kHz
G = 10		140			*			*		kHz
G = 100		25			*			*		kHz
G = 1000		2.5			*			*		kHz
Small Signal, ±1% Flatness										
G = 1		20			*			*		kHz
G = 10		10			*			*		kHz
G = 100		1			*			*		kHz
G = 1000		200			*			*		Hz
Full Power, G = 1 - 100		6.4			*			*		kHz
Slew Rate, G = 1 - 100	0.2	0.4		*	*		*	*		V/µsec
Settling Time (0.1%)										
G = 1		30	40		*	*		*	*	µsec
G = 100		40	55		*	*		*	*	µsec
G = 1000		350	470		*	*		*	*	µsec
Settling Time (0.01%)										
G = 1		30	45		*	*		*	*	µsec
G = 100		50	70		*	*		*	*	µsec
G = 1000		500	650		*	*		*	*	µsec

ELECTRICAL (CONT)

	INA104HP			INA104JP			INA104KP			
MODEL	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
OUTPUT AMPLIFIER, A_4										
OPEN-LOOP GAIN, $V_O = \pm 100$										
Rated Load $R_L \geq 2k\Omega$	100	115		*	*		*	*		dB
$R_L \geq 10k\Omega$	110	125		*	*		*	*		dB
RATED OUTPUT										
Voltage at $R_L = 2k\Omega$	10	12		*	*		*	*		V
$R_L = 10k\Omega$		12			*			*		V
Current	5	7.5		*	*		*	*		mA
Output Impedance		2			*			*		kΩ
Load Capacitance (unity-gain inverting)		2000			*			*		pF
Short Circuit Current		10			*			*		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			*			*		MHz
Full Power		9			*			*		kHz
Slew Rate	0.35	0.55		*	*		*	*		V/μsec
Settling Time										
0.1%		30			*			*		μsec
0.01%		40			*			*		μsec
INPUT OFFSET VOLTAGE										
Initial, $T_A = +25°C$		±1	±2		*	*		*	*	mV
vs Temp.		±5			*			*		μV/°C
INPUT BIAS CURRENT		+55	+150							nA
INPUT IMPEDANCE										
Differential		500			*			*		kΩ
Common-Mode		100			*			*		MΩ
RESISTORS, 10kΩ										
Accuracy		0.5	1.3		*			*		%
Drift		30	50		*	*		*	*	ppm/°C
Ratio Match		0.06	0.12		*	*		*	*	%
Drift		5			*			*		ppm/°C
INPUT VOLTAGE NOISE										
$f_B = 0.01Hz$ to $10Hz$		1.3			*			*		μV,p-p
Density										
$f_O = 10Hz$		22			*			*		$nV\sqrt{Hz}$
$f_O = 100Hz$		19			*			*		$nV\sqrt{Hz}$
$f_O = 1kHz$		17			*			*		$nV\sqrt{Hz}$
POWER SUPPLY, TOTAL										
Rated Voltage		±15			*			*		V
Voltage Range	±5		±20	*		*	*		*	V
Current, Quiescent		±8.1	±9.6		*	*		*	*	mA
TEMPERATURE RANGE										
Specification	0		+70	*		*	*		*	°C
Operation	-40		+85	*		*	*		*	°C
Storage	-40		+85	*		*	*		*	°C
θ_{J-C}		115			*			*		0°C/W
θ_{J-A}		350			*			*		0°C/W

*Specifications same as for INA104HP.

NOTES:
1. Typically the tolerance of R_G will be the major source of gain error. 2. Not including the TCR of R_G. 3. Adjustable to zero at any one gain.

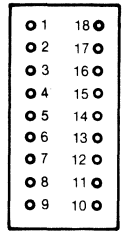
ABSOLUTE MAXIMUM RATINGS

Supply	±20V
Internal Power Dissipation	980mW
Input Voltage Range	±V_{CC}
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +85°C
Lead Temperature (soldering 10 seconds)	+300°C
Output Short-circuit Duration	Continuous to ground

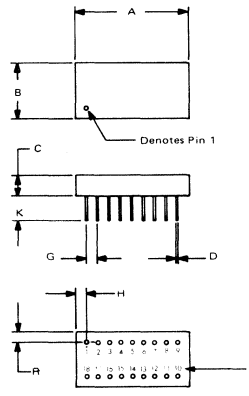
PIN DESIGNATIONS

1. GAIN SENSE
2. +IN
3. NEGATIVE SUPPLY
4. COMMON-MODE VOLTAGE SENSE
5. GAIN
6. COMMON
7. NONINVERTING INPUT TO A_4
8. OUTPUT OF A_3
9. FEEDBACK RESISTOR
10. OUTPUT OF A_4
11. FEEDBACK RESISTOR
12. SUMMING JUNCTION OF A_4
13. POSITIVE SUPPLY
14. GAIN
15. OFFSET ADJUST
16. OFFSET ADJUST
17. -IN
18. GAIN SENSE

(TOP VIEW)



MECHANICAL



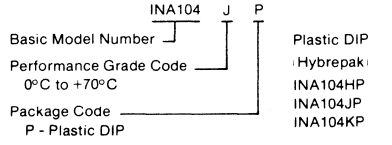
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.990	1.010	25.15	25.65
B	.490	.510	12.45	12.95
C	.190	.210	4.83	5.33
D	.018	.021	0.46	0.53
G	.100 BASIC		2.54 BASIC	
H	.080	.115	2.03	2.92
K	.130	.300	3.30	7.62
L	.300 BASIC		7.62 BASIC	
R	.080	.115	2.03	2.92

NOTE
Leads in true position within 0.01" (0.255mm) R at seating plane

Pin numbers shown for reference only

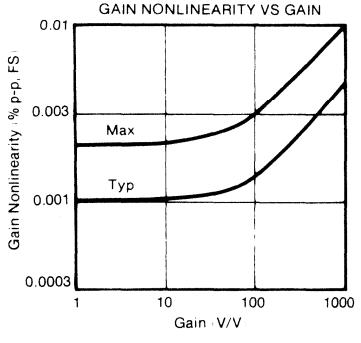
Numbers not marked on package

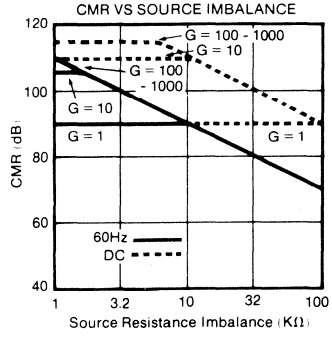
ORDERING INFORMATION

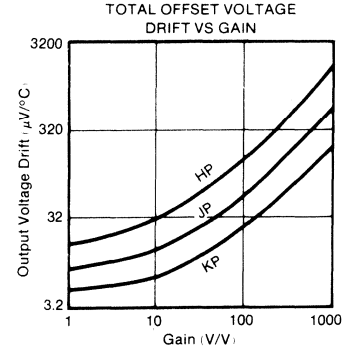


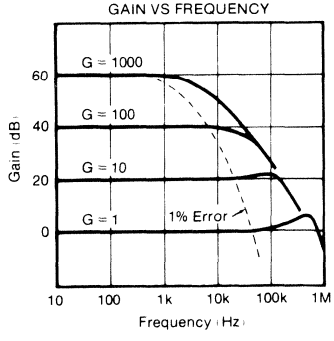
TYPICAL PERFORMANCE CURVES

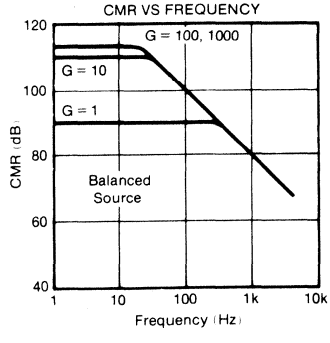
At +25°C, ±V_{CC} = 15VDC, and in circuit of Figure 1 unless otherwise specified.

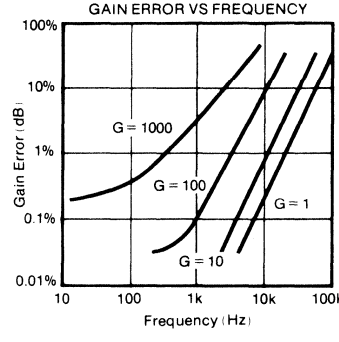


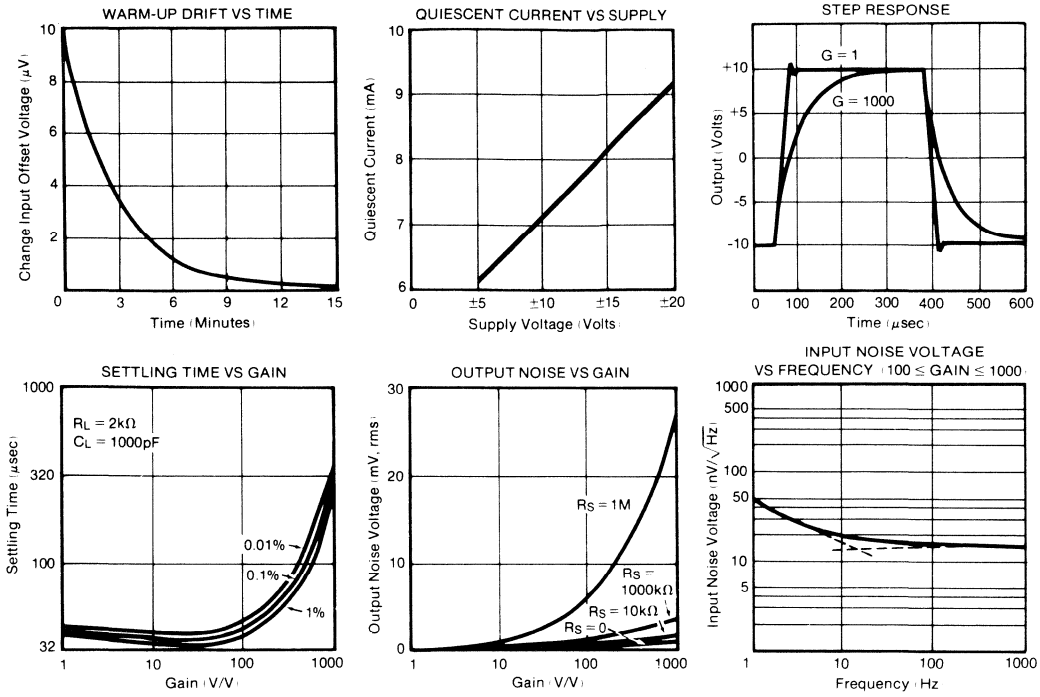












DISCUSSION OF PERFORMANCE

INSTRUMENTATION AMPLIFIERS

Instrumentation amplifiers are closed-loop gain blocks whose committed circuitry accurately amplifies the voltage applied to their inputs. They respond only to the difference between the two input signals and exhibit extremely-high input impedance, both differentially and common-mode. Feedback networks are packaged within the amplifier module. Only one external gain setting resistor must be added. An operational amplifier, on the other hand, is an open-loop, uncommitted device that requires external networks to close the loop. While operational amplifiers can be used to achieve the same basic function as instrumentation amplifiers, it is difficult to reach the same level of performance. Using operational amplifiers often leads to design trade-offs when it is necessary to amplify low level signals in the presence of common-mode voltages while maintaining high input impedances.

THE INA104

A simplified schematic of the INA104 is shown on the first page of this data sheet. It is a three-amplifier device which provides all the desirable characteristics of a premium performance instrumentation amplifier. In addition, it has features not normally found on integrated circuit instrumentation amplifiers.

The input section (A1 and A2) incorporates high performance, low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide the high input impedance ($10^{10}\Omega$) desirable in the instrumentation amplifier function. The offset voltage and offset voltage versus temperature is low due to the monolithic design and improved even further by the state-of-the-art laser-trimming techniques.

The output section (A3) is connected in a unity-gain difference amplifier configuration. A critical part of this stage is the matching of the four 10kΩ resistors which provide the difference function. These resistors must be initially well matched and the matching must be maintained over temperature and time in order to retain excellent common-mode rejection. (The 106dB minimum at 60Hz for gains greater than 100V/V is a significant improvement compared to most other integrated circuit instrumentation amplifiers.)

All of the internal resistors are compatible thin-film nichrome formed with the integrated circuit. The critical resistors are laser-trimmed to provide the desired high gain accuracy and common-mode rejection. Nichrome ensures long-term stability of trimmed resistors and simultaneous achievement of excellent TCR and TCR tracking. This provides gain accuracy and common-mode rejection when the INA104 is operated over wide temperature ranges.

The fourth op-amp (A4) of the INA104 adds a great deal of versatility and convenience to the amplifier. Its use allows easy implementation of active low-pass filtering, output offsetting, and additional gain generation. The pin connections make the use of this stage optional and the specifications appear separately in the table of Electrical Specifications.

USING THE INA104

Figure 1 shows the simplest configuration of the INA104. The gain is set by the external resistor, R_G, with a gain equation of $G = 1 + (40K / R_G)$. The reference and TCR of R_G contribute directly to the gain accuracy and drift.

For gains greater than unity, resistor R_G is connected externally between pins 5 and 14. At high gains where the value of R_G becomes small, additional resistance (i.e., relays, sockets) in the R_G circuit will contribute to a gain error. Care should be taken to minimize this effect. However, this error can be virtually eliminated with the INA104 by using the gain sense circuit connection.

Pins 1, 5, 14, and 18 are accessible so that a four-terminal connection can be made to R_G. (Pins 1 and 18 are the voltage sense terminals since no signal current flows into the operational amplifiers' inputs.) This may be useful at high gains where the value of R_G becomes small.

The optional offset null capability is shown in Figure 2. The adjustment affects only the input stage component of the offset voltage. Thus, the null condition will be disturbed when the gain is changed. Also, the input drift will be affected by approximately $0.31\mu V/^{\circ}C$ per $100\mu V$ of input offset voltage that is trimmed. Therefore, care should be taken when considering use of the control for removal of other sources of offset.

OPTIONAL OFFSET ADJUSTMENT PROCEDURE

It is frequently desirable to null the input component of offset (Figure 1) and occasionally that of the output

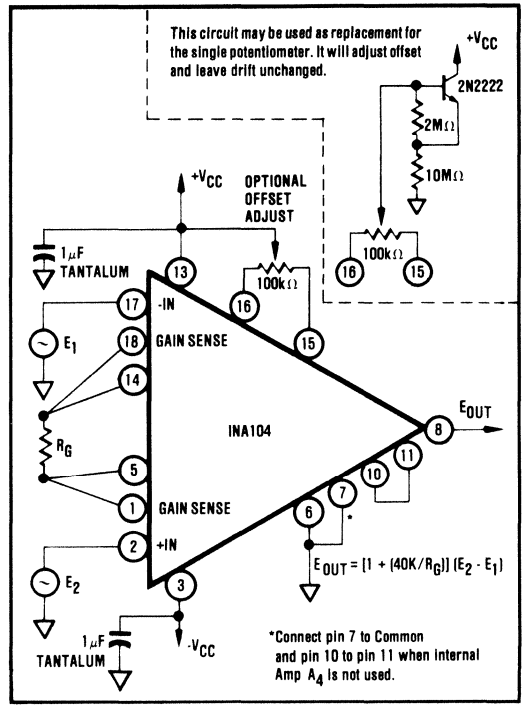


FIGURE 1. Basic Circuit Connection for the INA104 Including Optional Input Offset Null Potentiometer.

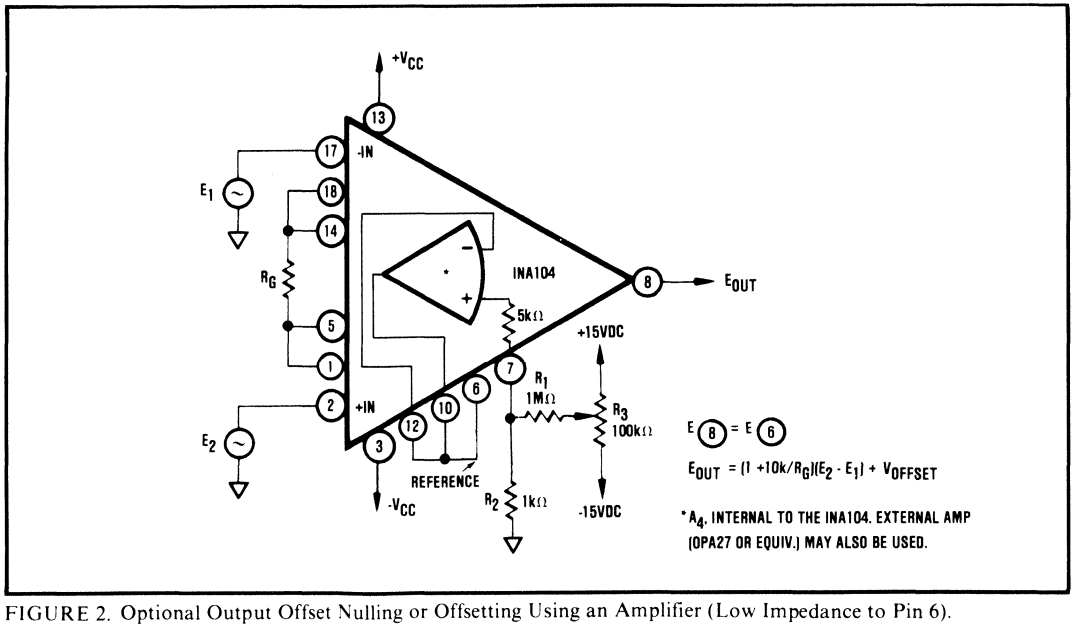


FIGURE 2. Optional Output Offset Nulling or Offsetting Using an Amplifier (Low Impedance to Pin 6).

(Figure 2). The quality of the potentiometer will affect the results, therefore, choose one with good temperature and mechanical-resistance stability. The procedure is as follows:

1. Set $E_1 = E_2 = 0V$ (be sure a good ground return path exists to the input).
2. Set the gain to the desired value by choosing R_G.
3. Adjust to 100Ω potentiometer in Figure 1 until the output reads 0V ±1mV or desired setting. Note that the offset will change when the gain is changed. If the output component of offset is to be removed or if it is desired to establish an intentional offset, adjust the 100kΩ potentiometer in Figure 2 until the output reads 0V ±1mV or desired setting. Note that the offset will not change with gain, but be sure to use a stable external amplifier with good DC characteristics. The range of adjustment is ±15mV as shown. For larger ranges change the ratio of R_1 to R_2. The op amp is used to maintain a low resistance (<0.1Ω) from pin 6 to Common to avoid CMR degradation.

BASIC CIRCUIT CONNECTION

The basic circuit connection for the INA104 is shown in Figure 1. The output voltage is a function of the differential input voltage times the gain.

Figure 1 does not include additional internal op amp A_4. Power supply bypassing with a 1μF tantalum capacitor or equivalent is always recommended.

In applications which do not use the fourth internal amplifier (A_4 - pins 7, 9, 10, 11, and 12), pin 7 should be connected to Common and pins 10 and 11 should be connected together. This will prevent the output of A_4 from saturating ("locking-up") and affecting the offset of the instrumentation amplifier, A_1, A_2, and A_3.

TYPICAL APPLICATIONS

Many applications of instrumentation amplifiers involve the amplification of low-level differential signals from bridges and transducers such as strain gages, thermocouples, and RTD's. Some of the important parameters include common-mode rejection (differential cancellation of common-mode offset and noise), input impedance, offset voltage and drift, gain accuracy, linearity, and noise. The INA104 accomplishes all of these with high precision.

Figures 3 through 13 show some typical applications circuits.

Figure 3 shows how the output stage may be used to provide additional gain. If gains greater than 1000V/V (10,000 up to 100,000 and greater) are desired it is better to place some gain in the output amplifier rather than the input stage due to the low values of R_G required ($R_G <$ 40Ω for $(1 + 40k/R_G) > 1000$). Note, however, that accuracy can degrade due to very-high amplification of offset, drift, and noise errors.

Output offsetting ("zero suppression" or "zero elevation") may be more easily accomplished with the INA104 than with most other IC instrumentation amplifiers as shown in Figure 4. The use of the extra internal op amp, A_4, means that CMR of the instrument amp is not disturbed, and that a convenient value of variable resistor can be used. The circuit shown in Figure 2 can also be used to achieve the desired offsetting by scaling the resistors R_1 and R_2. A low impedance path from pin 6 to Common should be provided to achieve the high CMR specified. Resistance above 0.1Ω will cause the CMR to fall below 106dB.

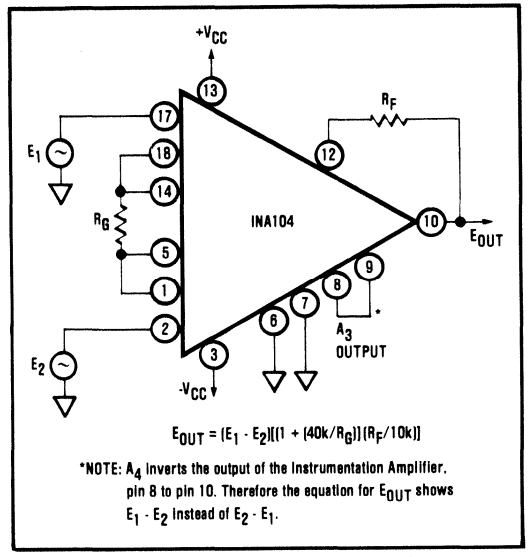


FIGURE 3. Additional Gain From Output Stage.

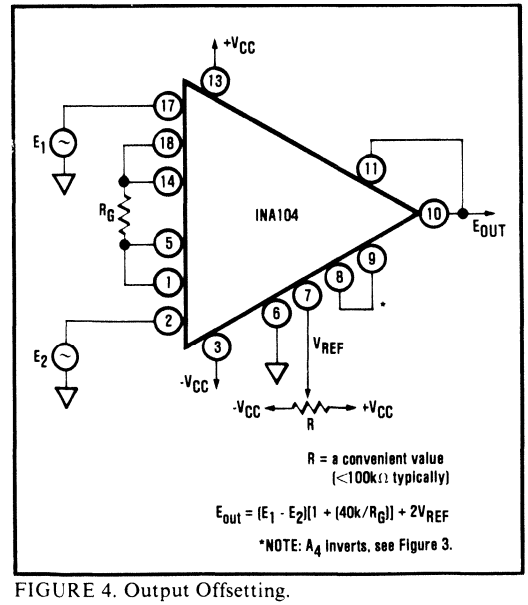


FIGURE 4. Output Offsetting.

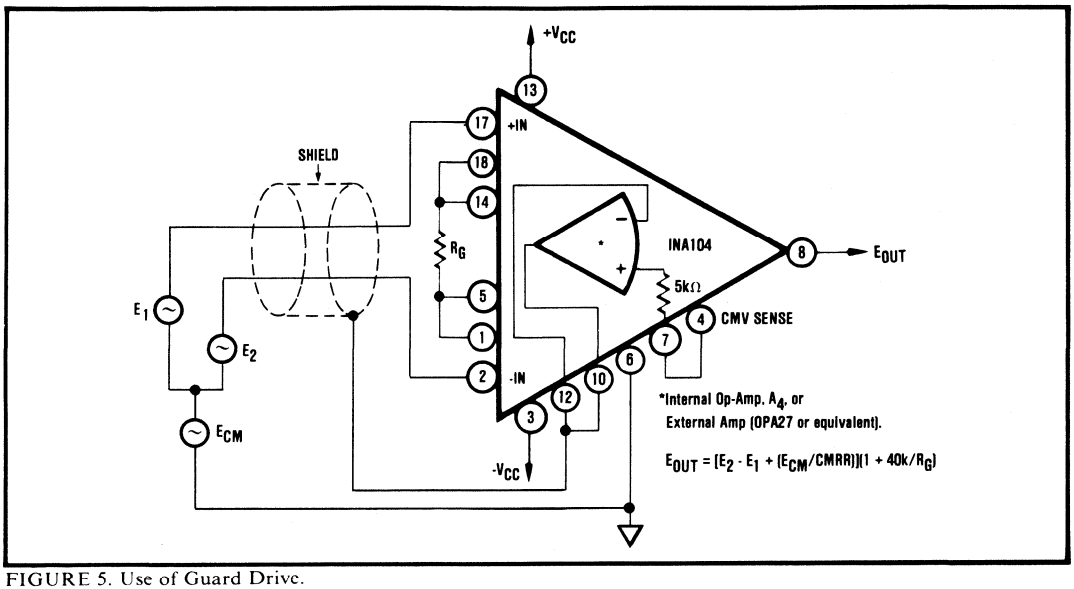


FIGURE 5. Use of Guard Drive.

Amplifier A_4 also allows active low-pass filtering to be implemented conveniently with a single capacitor. Filtering can be used for noise reduction or band-limiting of the output signal as shown in Figure 6.

The common-mode voltage from the 26kΩ resistors in the input section appears at pin 4. Figure 5 shows how this voltage can be used to drive the shield of the input cable. Since the cable is driven at the common-mode voltage, the effects of distributed capacitance is reduced and the AC system common-mode rejection may be improved. Amplifier A_4 buffers the CMV at pin 4 from the input cable.

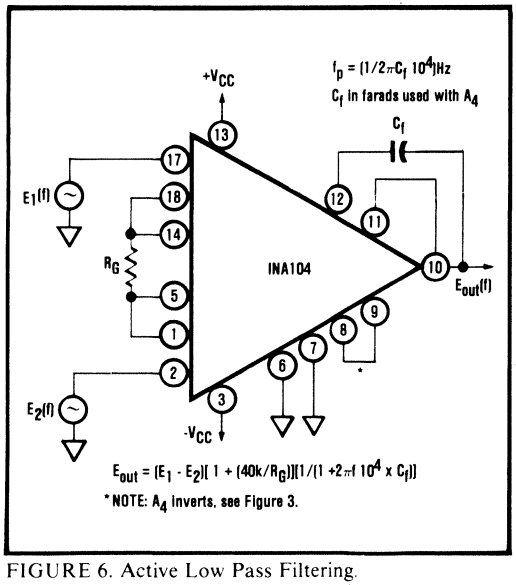


FIGURE 6. Active Low Pass Filtering.

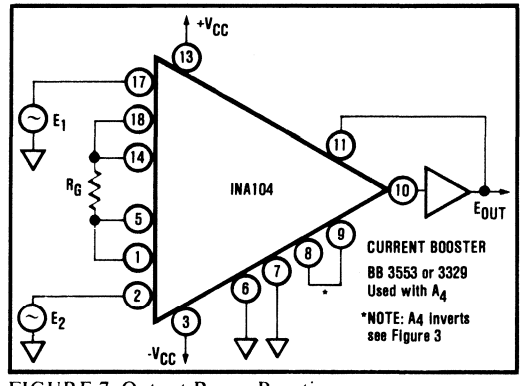


FIGURE 7. Output Power Boosting.

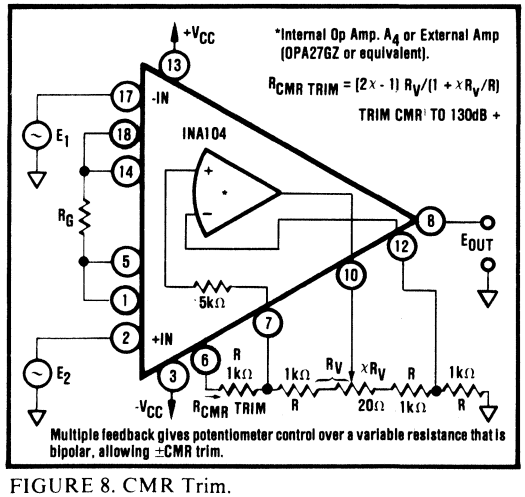


FIGURE 8. CMR Trim.

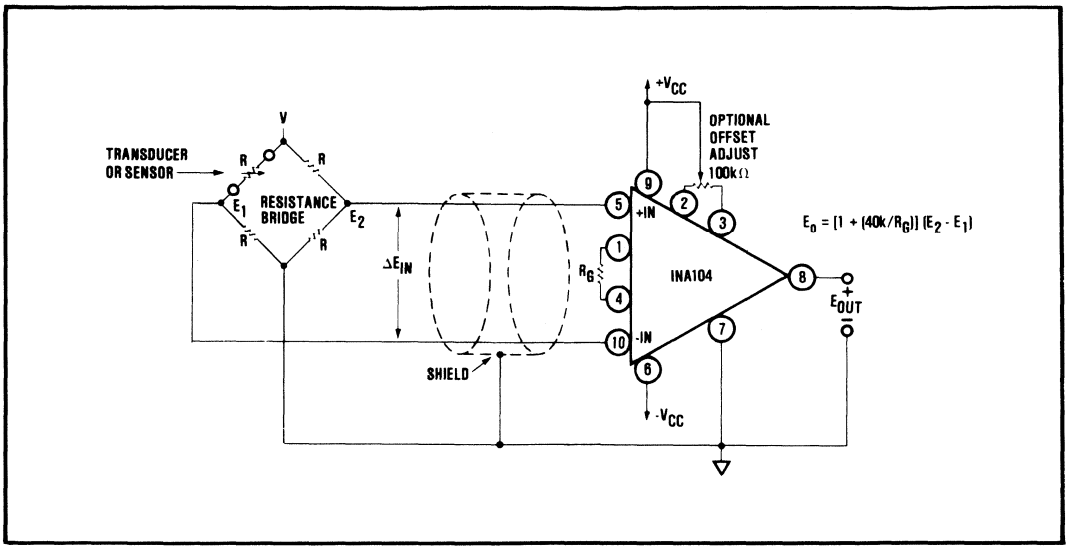


FIGURE 9. Amplification of a Differential Voltage from a Resistance Bridge.

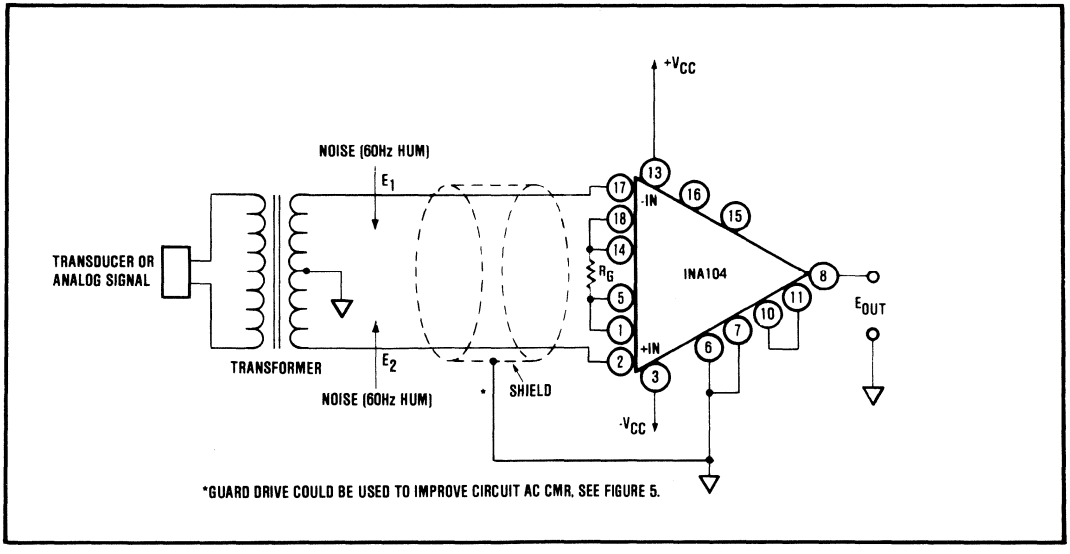


FIGURE 10. Amplification of a Transformer Coupled Analog Signal.

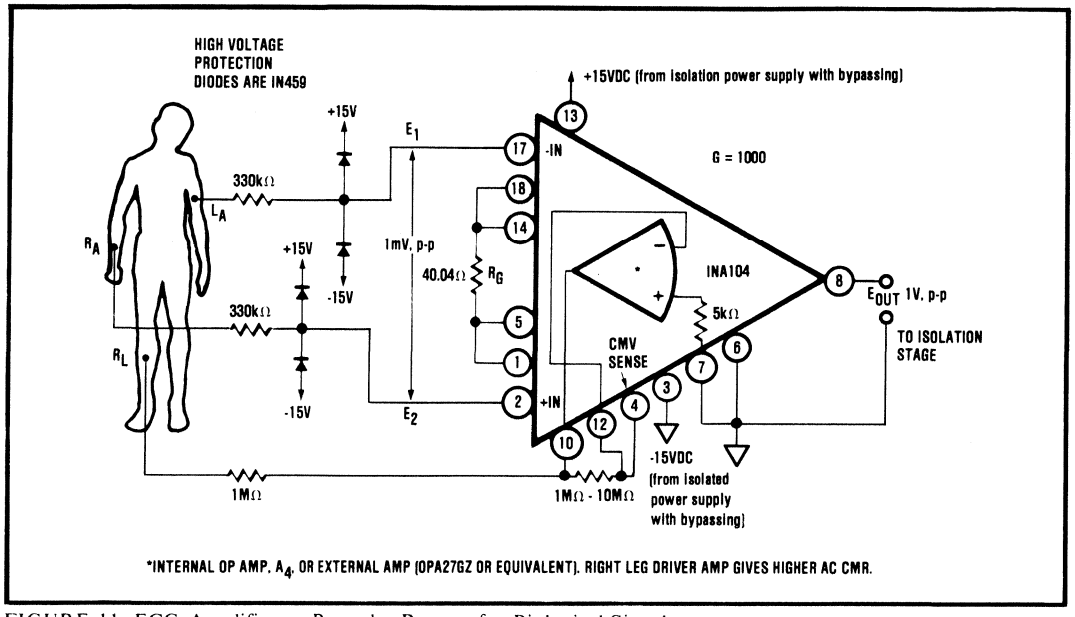


FIGURE 11. ECG Amplifier or Recorder Preamp for Biological Signals.

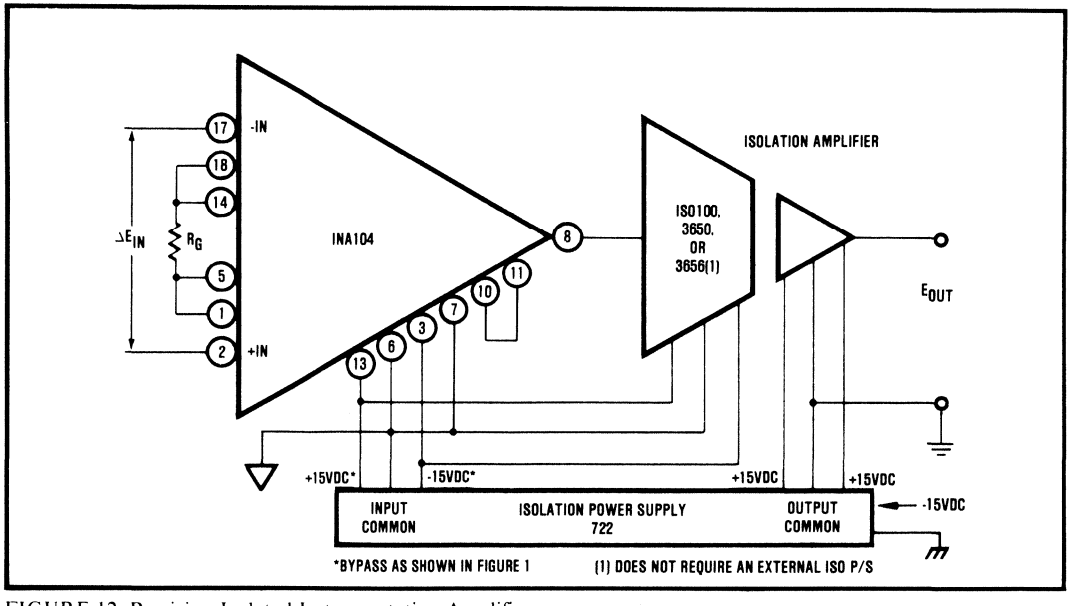


FIGURE 12. Precision Isolated Instrumentation Amplifier.

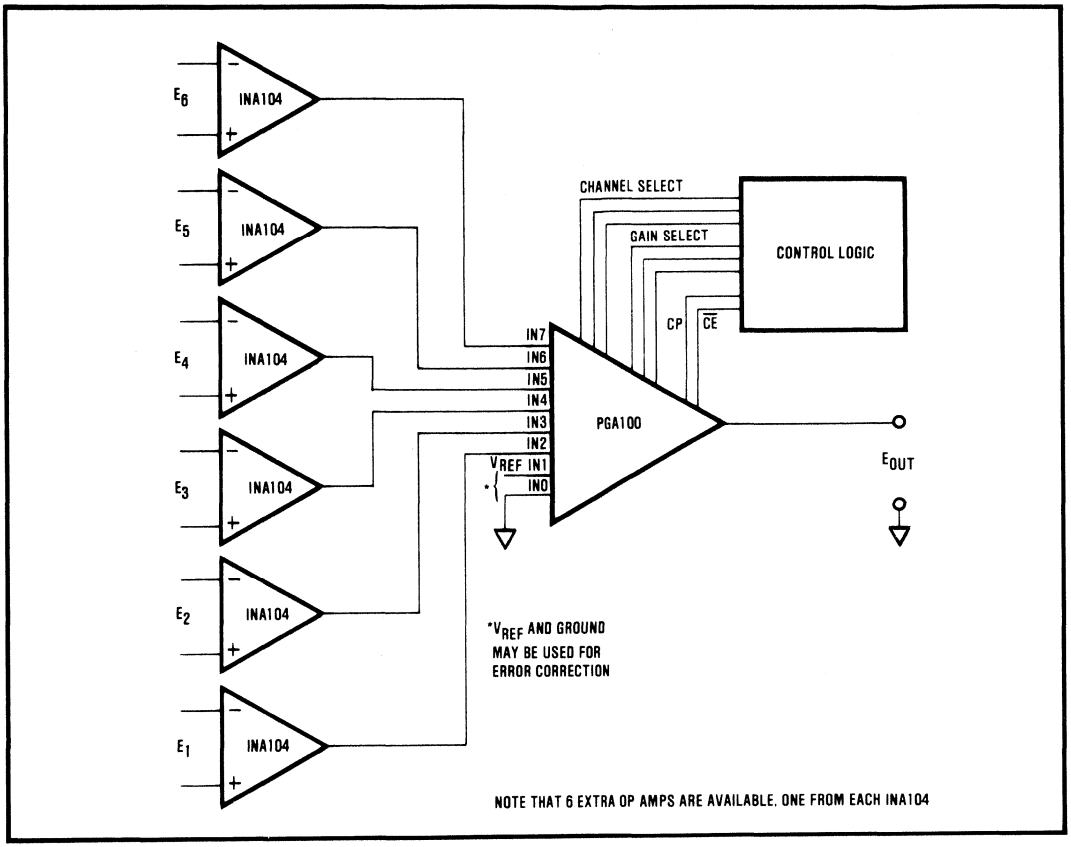


FIGURE 13. Multiple Channel Precision Instrumentation Amplifier.

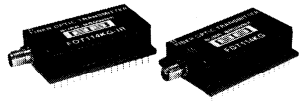
GENERAL RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damaging can cause performance degradation or failure, either immediate or latent. As a general practice we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove static-generating materials, such as untested plastics, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% is recommended).

BURR-BROWN®

FOT114



Analog Input Voltage-to-Frequency FIBER OPTIC TRANSMITTER

FEATURES

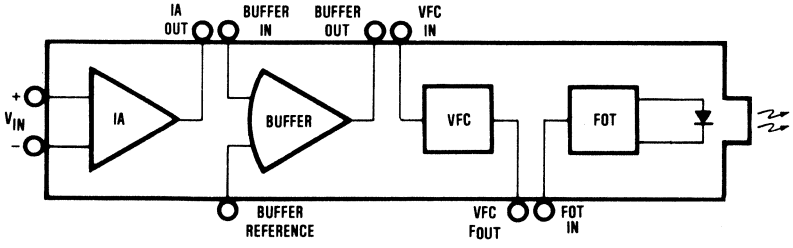
- ANALOG SIGNAL CONDITIONING
  Instrumentation amplifier input
  CMR of 106dB min at G = 1000
  Input impedance of $10^{10}\Omega$
- EXCELLENT DC LINEARITY (±0.05% max of FSR)
- LOW OFFSET DRIFT (±5ppm/FSR°C max)
- LONG DISTANCE OPERATION (up to 9.7km, IR version)
- IMMUNITY TO ELECTROMAGNETIC INTERFERENCE
- NO EXTERNAL RADIATED SIGNAL
- ELECTRICAL ISOLATION

APPLICATIONS

- REMOTE INSTRUMENTATION SYSTEMS
- INDUSTRIAL PROCESS CONTROL
- POWER PLANT CONTROL
- MEDICAL MONITORING
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- LOW COST ANALOG-TO-DIGITAL CONVERSION
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY

DESCRIPTION

The FOT114 is a versatile, self-contained, analog-input hybrid fiber optic transmitter. When connected to a suitable fiber optic cable and receiver, it is capable of transmitting analog input signals as small as 10mV full scale for distances up to 2.4km with a typical linearity error of ±0.02%. Furthermore, the infrared (IR) version can transmit over link lengths as long as 9.7km. The FOT114 contains a precision instrumentation amplifier (IA), uncommitted buffer, voltage-to-frequency converter (VFC), and fiber optic transmitter section (FOT). The IA provides high input impedance of $10^{10}\Omega$, CMR of 106dB (gain = 1000), and resistor-programmable gain from 1V V to 1000V V. The buffer allows level shifting which is useful for accommodating bipolar signals or offset-ting unipolar signals. The VFC linearly converts input voltages between 0 to +10V to an adjustable pulse train ranging from 0 to 100kHz. The FOT drives the output LED at pin-programmable power levels. Output power is specified as actual power launched.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $\pm V_{CC}$ = 15VDC and V_{DD} = +5VDC unless otherwise noted.

MODEL		FOT114KG			FOT114KG-IR			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSFER FUNCTION(1)				$G_T = G_{IA} \times G_{VFC}$				Hz/V
INSTRUMENTATION AMPLIFIER SECTION								
Transfer Function			$G_{IA} = I_{AOUT}/\Delta V_{IN} = 1 + (40K/R_G)$					V/V
Gain Range		1		1000	*		*	V/V
Gain Error in Transfer Function			$\pm(0.04 + 0.000016G - (0.02/G))$ typ; $\pm(0.1 + 0.003G - (0.05/G))$ max					% of FS
Gain Nonlinearity, DC			$(\pm 0.002 + 10^{-5}G)$ typ; $(\pm 0.005 + 2 \times 10^{-5}G)$ max					% p-p, FS
Gain Temperature Coefficient	R_G TCR = 0							
	G = 1		±2	±5		*	*	ppm/°C
	G = 10		±20	±100		*	*	ppm/°C
	G = 100 to 1000		±22	±110		*	*	ppm/°C
Rated Output Voltage		±10	±12.5		*	*		V
Rated Output Current		±5	±12.5		*	*		mA
Output Impedance	G = 1000		0.01			*		Ω
Input Impedance								
Differential			$10^{10} \parallel 3$			*		Ω || pF
Common-Mode			$10^{10} \parallel 3$			*		Ω || pF
Input Voltage Range(2)		±10	±12		*	*		V
Common-Mode Rejection								
with 1kΩ Source Imbalance	G = 1	80	90		*	*		dB
	G = 10	96	106		*	*		dB
	G = 100 to 1000	106	110		*	*		dB
Input Offset Voltage								
Initial			$\pm 25 \pm (200/G)$	$\pm 50 \pm (600/G)$		*	*	µV
vs Temperature				$\pm 2 \pm (20/G)$			*	µV/°C
vs Supply			$\pm(1 + (20/G))$	$\pm(2 + (100/G))$		*	*	µV/V
vs Time			$\pm(1 + (20/G))$	$\pm(2 + (40/G))$		*	*	µV/mo
Input Bias Current								
Initial, each input			±15	±50		*	*	nA
vs Temperature			±0.3			*		nA/°C
vs Supply			±0.1			*		nA/V
Input Offset Current								
Initial			±15	±50		*	*	nA
vs Temperature			±0.5			*		nA/°C
Input Noise Voltage	f_B = 0.1Hz to 10Hz		0.8			*		µV, p-p
Input Noise Voltage Density	G = 100							
	f_O = 10Hz		17.9			*		$nV/\sqrt{Hz}$
	f_O = 100Hz		15.3			*		$nV/\sqrt{Hz}$
	f_O = 1000Hz		12.7			*		$nV/\sqrt{Hz}$
Input Noise Current	f_B = 0.1Hz to 10Hz		50			*		pA, p-p
Input Noise Current Density	f_O = 10Hz		0.8			*		$pA/\sqrt{Hz}$
	f_O = 100Hz		0.46			*		$pA/\sqrt{Hz}$
	f_O = 1000Hz		0.35			*		$pA/\sqrt{Hz}$
Small Signal Flatness, ±3dB	G = 1		300			*		kHz
	G = 10		140			*		kHz
	G = 100		25			*		kHz
	G = 1000		2.5			*		kHz
Small Signal Flatness, ±1dB	G = 1		20			*		kHz
	G = 10		10			*		kHz
	G = 100		1			*		kHz
	G = 1000		0.2			*		kHz
Full Power Bandwidth	G = 1 to 100		6.4			*		kHz
Slew Rate	G = 1 to 100	0.2	0.4		*	*		V/µsec
Settling Time to 0.1%(3)	G = 1		30			*		µsec
	G = 100		40			*		µsec
	G = 1000		350			*		µsec
Settling Time to 0.01%(3)	G = 1		30			*		µsec
	G = 100		50			*		µsec
	G = 1000		500			*		µsec
BUFFER SECTION								
Gain		-0.999	-1	-1.001	*	*	*	V/V
Input Offset Voltage			±1			*		mV
Input Bias Current				150			*	nA
Output Current		10			*			mA

ELECTRICAL (CONT)

At T_A = +25°C, ±V_{CC} = 15VDC and V_{DD} = +5VDC unless otherwise noted.

MODEL		FOT114KG			FOT114KG-IR			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
VOLTAGE-TO-FREQUENCY CONVERTER SECTION								
Transfer Function			$G_{VFC} = [132 \times 10^{-3}/[(C_1 + 330 \times 10^{-12})(R_1 + 40 \times 10^3)]$					Hz/V
Gain Error (adjustable to zero)			±0.1	±0.5		*	*	% of FS
Linearity Error	100Hz < f_{out} < 100kHz		±0.02	±0.05		*	*	% of FS
Power Supply Sensitivity	12V ≤ V_{CC} ≤ 18V		0.003	0.015		*	*	% of FS/%
Input Voltage Range[4]		0		+10	*		*	V
Input Current Range[4]		0		+0.25	*		*	mA
Input Impedance		32	40		*	*		kΩ
Input Offset Voltage (adjustable to zero)[4]			±0.1	±0.5		*	*	mV
Full Scale Drift (offset & gain)	+25°C to +70°C		±15	±70		*	*	ppm/°C
	0°C to +25°C		±100	±175		*	*	ppm/°C
Input Offset Drift	0°C to +70°C		±2	±5		*	*	ppm of FSR/°C
Settling Time (to within linearity spec.)		1 pulse of new freq. plus 1 µsec				*		
OPTICAL OUTPUT SECTION								
Output Power, Launched[5][6]								
Peak, Normal VFC Operation	200µm, 0.48NA	15	30		150	300		µW
		-18.2	-15.2		-8.2	-5.7		dBm
Continuous[7]		5	10		50	100		µW
		-23	-20		-13	-10.5		dBm
Output Power, Total			90			600		µW
			-10.5			-2.2		dB
Output Power Adjust Range[5]	max to min		15			*		dB
Wavelength, LED	P_O max	650	665	680	850	880	910	nm
Spectral Half-Width	-3dB from P_O max		25			80		nm
Fiber Pigtail Core Diameter			375			*		µm
Fiber Pigtail NA	-10dB		0.66			*		
Rise Time, t_R			150			600		nsec
Fall Time, t_F			150			600		nsec
FOT Input	See Figure 7							
Input "High" Voltage	$I_{FOT\ IN}$ = 7.5mA		+1.4			*		V
Input "Low" Voltage				+0.4			*	V
Allowable Input "High" Current	PWR SEL, 0dB	7.5		20	*		*	mA
	PWR SEL, -6dB	2		20	*		*	mA
Baud Rate (digital)	NRZ, P_O max	0 to 2M	0 to 4M		0 to 0.75M	0 to 1M		Baud
POWER SUPPLY								
Rated Voltage V_{CC}/V_{DD}			±15/+5			*		V
Voltage Range V_{CC}/V_{DD}		±9/+4.5		±20/+20	*		*	V
Current, Quiescent								
Analog, V_{CC}			+20, -14			*		mA
Digital, V_{DD}	Avg at 25% duty cycle							
	LED OFF		0.1			*		mA
Avg/peak	LED ON, PWR SEL, -15dB		+3.1/+12.5			*		mA
Avg/peak	LED ON, PWR SEL, 0dB		+95/+375			*		mA
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Operation		-40		+70	*		*	°C
Storage		-55		+85	*		*	°C

*Specifications same as FOT114KG

NOTES:
1. Total transfer function is adjustable and is nominally 10kHz/V. The VFC duty cycle is nominally 25% at full scale.
2. IA is capable of ±10V input. VFC is limited to 0 to +10V input. To convert bipolar inputs to unipolar the buffer amplifier reference is shifted.
3. For low IA gains, VFC settling time is predominant.
4. Negative VFC inputs can cause VFC input offset voltage shifts.
5. Optical output power is adjustable. See the Applications Section. Optical power is measured into an exit numerical aperature (NA) of 0.48 and a core diameter of 200µm. For other cable core diameters and NA see Typical Performance Curves and Cable Selection Section.
6. The IR version offers increased optical power and longer links.
7. When directly using the FOT input control (FOT IN), the maximum allowable LED power is -6dB for duty cycles greater than 25%.

ABSOLUTE MAXIMUM RATINGS

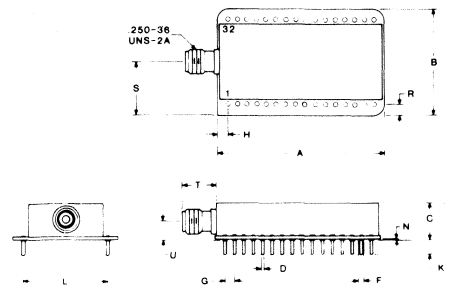
±V_{CC}	20VDC
V_{DD}	+20VDC
Input Voltage Range	±20VDC
FOT IN Current	20mA
FOT IN Duty Cycle with 0dB Power Select	25%
Storage Temperature Range	-55°C to +85°C
Operating Temperature Range	-40°C to +70°C
Lead Temperature (soldering 10 seconds)	+300°C

PIN CONFIGURATION

1. Pulse Width	32. NC*
2. VFC V_{IN}	31. NC*
3. VFC Comparator In	30. Analog Common
4. VFC Integrator Out	29. IA Out
5. VFC I_{IN}	28. Buffer Reference
6. +V_{CC}	27. Buffer In
7. VFC F_{OUT}	26. Buffer Out
8. FOT IN	25. -V_{CC}
9. Digital Common	24. +V_{IN}
10. -3dB	23. Gain Sense
11. -3dB	22. R_G (Gain Set)
12. -6dB	21. Offset Trim
13. -9dB	20. Offset Trim
14. -12dB	19. R_G (Gain Set)
15. -15dB	18. Gain Sense
16. V_{DD}	17. -V_{IN}

*No Internal Connection.

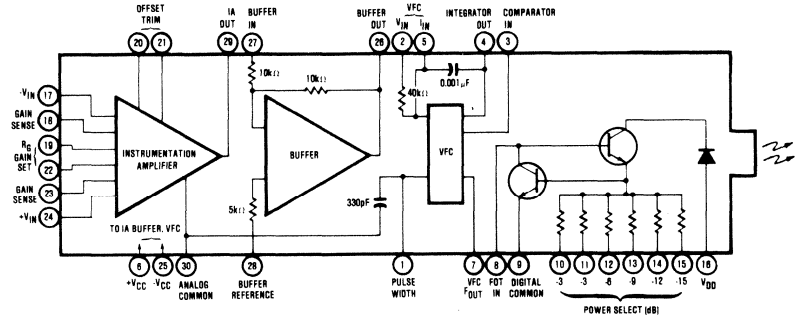
MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.710	1.750	43.43	44.46
B	1.106	1.140	28.09	28.96
C	.370	.430	9.40	10.92
D	.016	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30
S	.530	.590	13.46	14.99
T	.345	.355	8.76	9.02
U	.192	.220	4.88	5.59

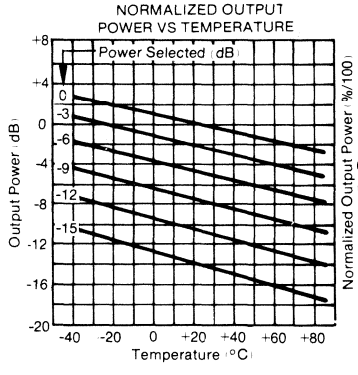
NOTES:
1. Leads in True Position within 0.10" (0.25mm) R at Seating Plane.
2. Pin Numbers shown for Reference Only. Numbers may not be marked on package.

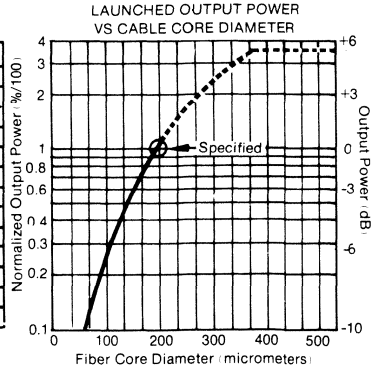
CONNECTION DIAGRAM

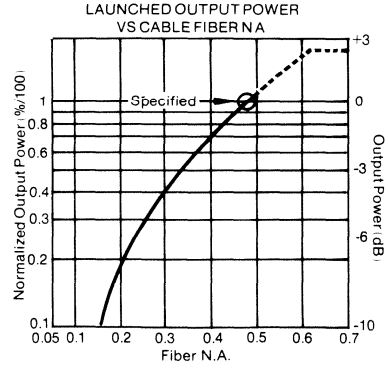


TYPICAL PERFORMANCE CURVES

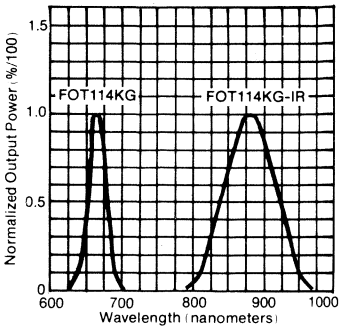
(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} +5V, unless otherwise noted.)



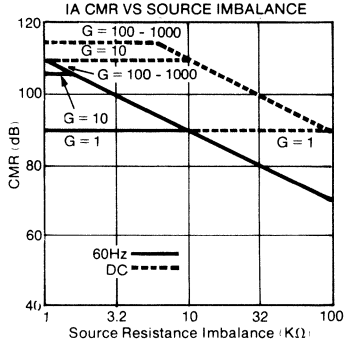




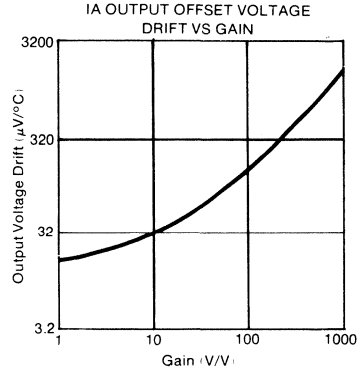
TRANSMITTER SPECTRAL OUTPUT



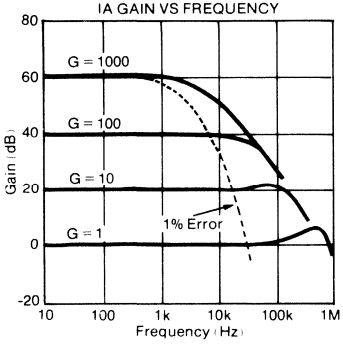
IA CMR VS SOURCE IMBALANCE



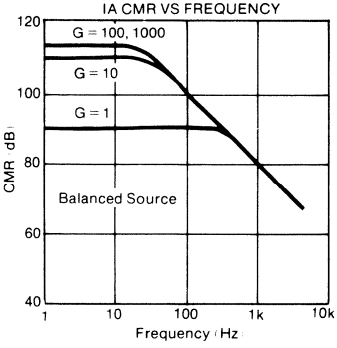
IA OUTPUT OFFSET VOLTAGE DRIFT VS GAIN



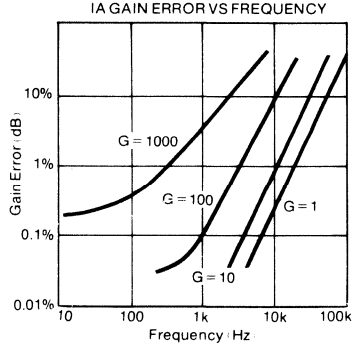
IA GAIN VS FREQUENCY



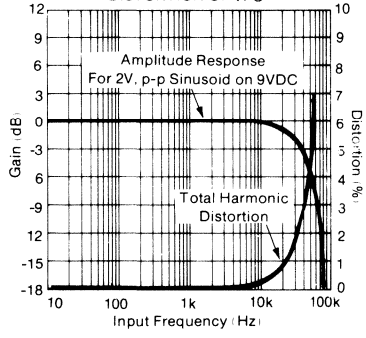
IA CMR VS FREQUENCY



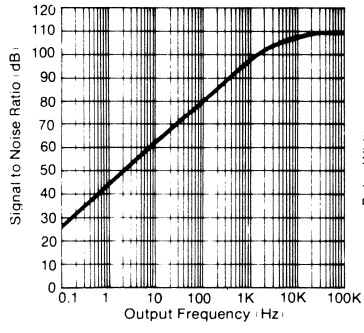
IA GAIN ERROR VS FREQUENCY



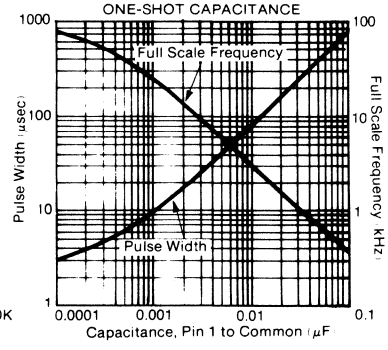
BANDWIDTH AND DISTORTION OF VFC



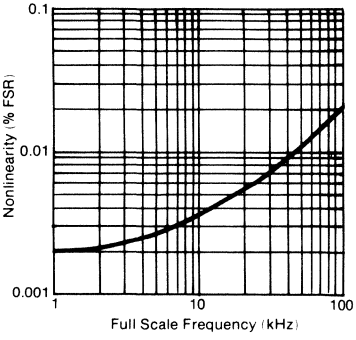
SIGNAL TO NOISE RATIO VS FREQUENCY
(gain = 5kHz/V)



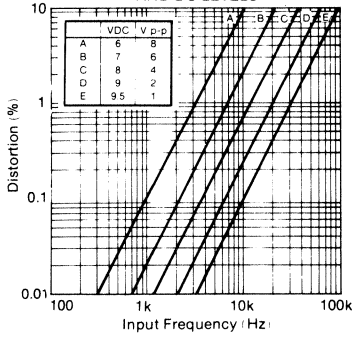
OUTPUT PULSE WIDTH AND FULL SCALE FREQUENCY VS EXTERNAL ONE-SHOT CAPACITANCE



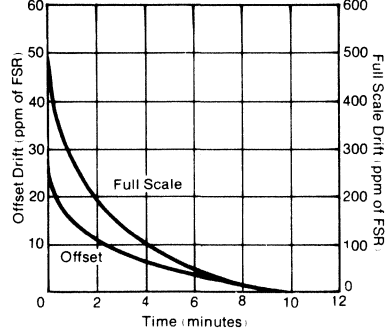
LINEARITY ERROR VS FULL SCALE FREQUENCY



DISTORTION VS INPUT FREQUENCY FOR VARIOUS INPUT AMPLITUDES AND DC LEVELS



OFFSET AND FULL SCALE WARM-UP DRIFT VS TIME



THEORY OF OPERATION

The block diagram of the FOT114 is shown on the front page of this data sheet. It consists of an instrumentation amplifier, buffer, voltage-to-frequency converter, and a fiber optic transmitter which are individually accessible and specified separately to afford maximum versatility to the user.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier (IA) is composed of three compatible thin-film op amps and has the advantage of high impedance, superior CMR, high gain accuracy, and excellent drift performance. The gain is set by a single resistor (R_G) and is described by the equation $G = 1 + (40k/R_G)$. A low TC resistor should be used for R_G because it contributes directly to the gain drift. The Gain Sense lines on pins 18 and 23 are connected directly across R_G and eliminate gain error due to wiring. The Offset Trim pins 20 and 21 may be connected as shown in Figure 1. However, since this adjustment affects only the input stage component of offset, the null condition will be disturbed when the gain is changed. Additionally, the input drift will be affected by approximately $0.33\mu V/°C$ per $100\mu V$ of input offset nulled. By performing the offset adjust on the VFC at pin 5, as shown in Figure 3, both of these effects can be avoided. Some resistance path to ground must be provided for the IA input bias currents (pins 17 and 24). For floating inputs, a $1M\Omega$ resistor can typically be used, but any value up to $50M\Omega$ is acceptable. This IA is similar to the Burr-Brown INA101AM.

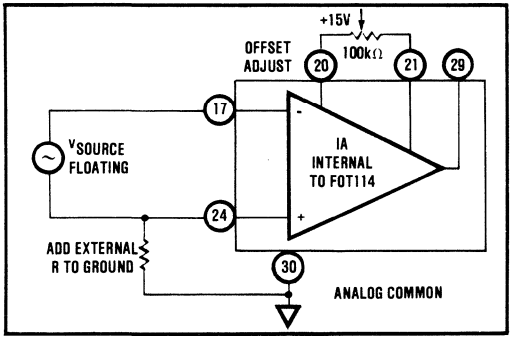


FIGURE 1. Instrumentation Amplifier with Offset Adjust and External Resistor for Floating Source.

VOLTAGE-TO-FREQUENCY CONVERTER

The VFC section is a monolithic voltage-to-frequency converter with excellent linearity and stability. It produces a digital pulse train output at pin 7 with a repetition rate directly proportional to the analog input voltage level at pin 2. This output is ideally suited for fiber optic transmission. The VFC is composed of an integrator, comparator, one-shot capacitor and 1mA current sink. The integrator produces a two-part ramp. The first part is a function of the input voltage and the second part is dependent on both the input voltage and current sink. The one-shot fires when the initial ramp reaches approximately 0V and lasts for a period determined by the pulse width capacitor and internal reference. The output will ramp back up by the current sink until the one-shot period ends. The process then repeats. The full scale frequency may be lowered by adding capacitance from pin 1 to ground, and the gain can be changed by adding a resistor in series with pin 2. (See Gain and Offset and Full Scale Frequency Adjustment Sections). A lower full scale frequency results in a lower linearity error. This VFC is similar to the Burr-Brown VFC32BM.

FIBER OPTIC TRANSMITTER

The FOT section drives the LED at a pin-programmable current level. The current is established by the resistor placed across a base emitter voltage of approximately 0.65V. To select a particular output power, the desired power select pin is connected to Digital Common.

MINIMAL CONNECTIONS

In many applications the FOT114 will require no adjustments. This is due to active laser-trimming of both IA and VFC gain and offset parameters. Figure 2 shows the minimal connections required for a usable transmitter circuit. Notice there are no external components. The full scale VFC gain error will be 0.5% max, and the VFC offset will be 0.5mV max. These are predominant over the IA.

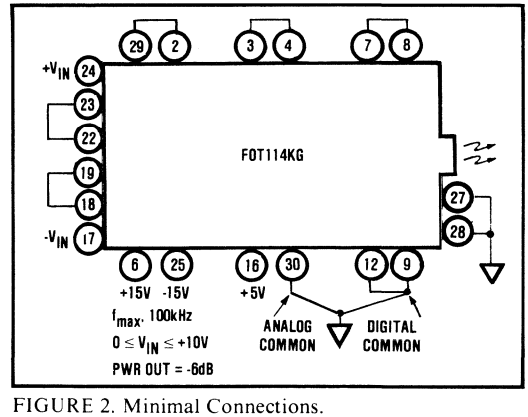


FIGURE 2. Minimal Connections.

OPTICAL POWER ADJUSTMENT

The LED current and, hence, optical power is set by connecting one or more of the power select pins to Digital Common. Maximum power (0dB) is selected by connecting both -3dB pins (10 and 11) to Digital Common. 0dB should be used only when the FOT is driven in pulsed mode of 25% duty cycle or less which is guaranteed when driven by the VFC. The power select pins provide a highly accurate selection of LED current; however, due to the nonlinear characteristics of the LED the optical output power does not vary directly as the drive current.

Table I shows the typical variation in optical output power versus current.

TABLE I. Optical Output Power versus Current.

Power Selected	LED Current	Min Output Power, +25°C	
(dB)	(mA)	visible (μW)	IR (μW)
-15	12.5	0.85	8.5
-12	25	1.6	16
-9	50	2.8	28
-6	100	5	50
-3*	200	8.5	85
0**	375	15	150

*50% max duty cycle **25% max duty cycle

GAIN AND OFFSET ADJUSTMENT

Overall gain is defined in terms of frequency out divided by voltage in. The general transfer function of Figure 3 is:

$$G_1 = \frac{F_{OUT}}{V_{IN}} = \frac{132 \times 10^{-3}[1 + (40 \times 10^3 R_G]}{(C_1 + 330 \times 10^{-12})(R_2 + 40 \times 10^3)} \text{ in Hz/V} \quad (1)$$

where,

$1 + (40 \times 10^3 R_G) = G_{IA}$ = Instrumentation Amplifier Gain.

$(C_1 + 330 + 10^{-12})$ = VFC total one-shot capacitance.

$(R_2 + 40 \times 10^3)$ = VFC total gain setting resistance. Note the $40 \times 10^3 \Omega$ resistor may be paralleled with a 3.9MΩ resistor (pins 2 and 5) as in Figure 3.

R_G = external IA gain setting resistor in ohms between pins 19 and 22.

C_1 = external one-shot capacitor in farads between pins 1 and 30.

R_2 = external VFC gain setting resistor in ohms between pins 29 and 2.

If gain and offset adjustments are necessary, they may be done either on the IA or the VFC; however, if different gains are selected, these adjustments are most easily made on the VFC. Figure 3 shows how to connect potentiometers for VFC gain and offset adjustment. The gain is adjusted by connecting a fixed resistor or potentiometer, R_2, from pin 29 to pin 2. This is in series with the parallel combination of R_4 and the internal 40kΩ resistor. R_2 then has an adjustment range of approximately ±1% which is ample to null the ±0.5%, maximum gain error of the VFC. The offset is typically adjusted by injecting a small current into the VFC summing junction (VFC I_{IN}) by connecting a 10kΩ to 100kΩ potentiometer, R_1, and 10MΩ resistor to pin 5.

Null the offset and gain by the following calibration procedure:

1. Apply a DC input voltage to produce an output frequency of 0.001 x full scale.
2. Adjust R1 for the proper output frequency at pin 7.
3. Apply a DC input voltage to produce a full scale output frequency.
4. Adjust R2 for the proper full scale output at pin 7.
5. Iterate as necessary.

Once the gain error is zeroed, IA gain may be changed while maintaining a very high overall gain accuracy. R_G then sets the gain according to the equation:

$$G_{IA} = 1 + (40k\ R_G) \quad (2)$$

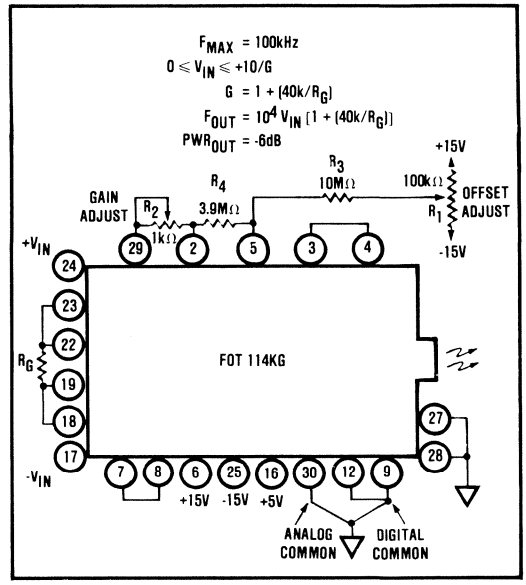


FIGURE 3. Basic Circuit Connection for Gain and Offset Adjustment.

FULL SCALE FREQUENCY ADJUSTMENT

The full scale frequency of the FOT114 may be reduced to improve linearity (the typical nonlinearity with a 10kHz full scale is 0.003% FSR) or to make the transmitter compatible with lower speed receivers. Two external capacitors shown in Figure 4 are chosen as follows:

$$C_1 = (33 \times 10^{-6})\ f_{MAX} - 3.30 \times 10^{-10} \text{ farads} \quad (3)$$

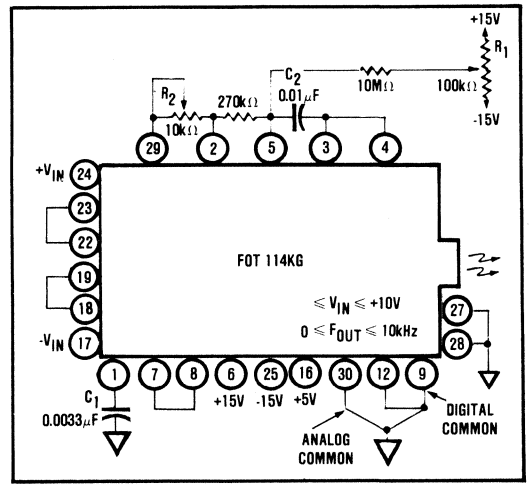


FIGURE 4. 10kHz Full Scale Connection.

Select the closest standard value to the capacitance given by the equation. A low drift capacitor such as an NPO ceramic or silver mica type is recommended. The initial tolerance is not critical since R_2 will be adjusted to remove initial gain errors.

$$C_2 = (10^{-4}\ f_{MAX}) - 1.0 \times 10^{-9} \text{ farads} \quad (4)$$

Select one for low leakage and low dielectric absorption. A mylar or polycarbonate type is recommended.

CURRENT INPUT CONNECTION

A current input can be achieved, as shown in Figure 5, by injecting a current into the VFC integrator summing junction, pin 5.

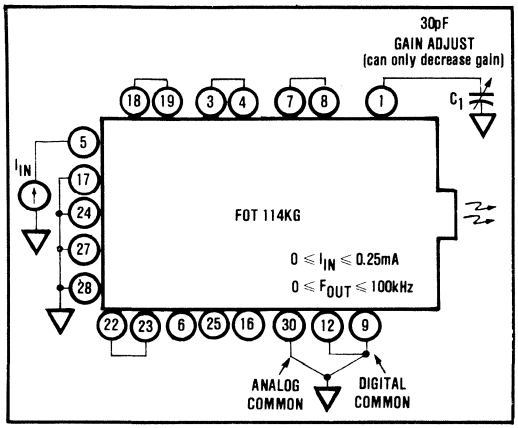


FIGURE 5. Current Input Connection.

BIPOLAR INPUT CONNECTION

A bipolar input can be accommodated by offsetting the buffer as shown in Figure 6. This connection is necessary because the VFC can accept only positive inputs. The effective offset is twice the voltage applied to pin 28. The buffer reference source impedance should be less than 100kΩ.

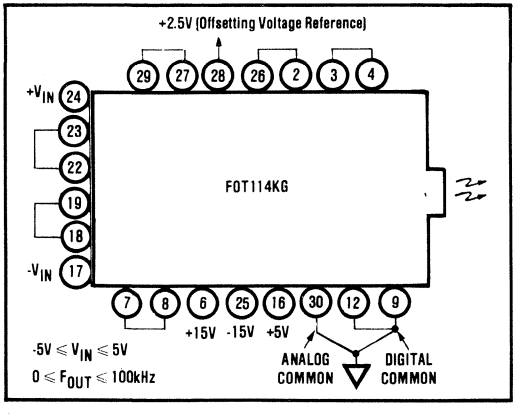


FIGURE 6. Bipolar Input Connection.

DIGITAL TRANSMITTER OPERATION

Figure 7 shows an interface circuit for logic input operation. TTL or CMOS can be accommodated at the interface input, however, the current drive into pin 8 should be limited (see Electrical Specifications).

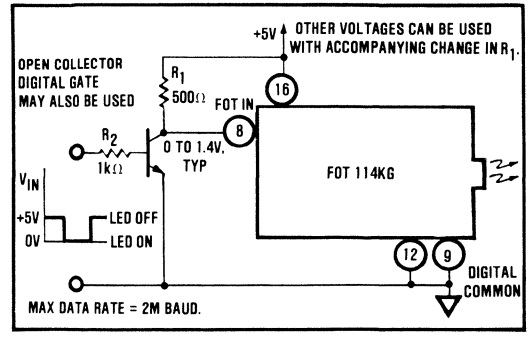


FIGURE 7. Digital Input Connection.

CABLE SELECTION

The FOT114/FOR110 connector is compatible with Amphenol 905 and 906 series or similar SMA connectors and can be used with a wide variety of cable types. The choice of a cable type depends on the particular application.

The visible (665nm) output of the FOT114KG is well matched for use with low cost all-plastic cable as well as glass and silica fibers. The high power infrared (880nm) output of the FOT114KG-IR provides improved performance with glass and silica fibers. However, use with plastic fibers is severely limited due to high attenuation of these materials in the infrared.

The operating temperature range and mechanical integrity of fiber optic cables vary widely. Consult manufacturers' specifications for specific information; some are shown in Table II. Table III contains calculated link performance for selected fiber optic cables. Performance is based on best available data from fiber optic cable manufacturers at time of printing.

The transmitter output power is specified as the power coupled into a 200μm core diameter fiber with an NA of 0.48. Larger NA (up to 0.66) couples more power, and smaller NA less power. Larger core diameter (up to 375μm) couples more power and smaller core diameter couples less power.

Power coupled into various cables can be calculated as follows:

Power coupled into cable =

$$\left(\frac{\text{Dia.}}{200\mu\text{m}}\right)^2 \times \left(\frac{NA}{0.48}\right)^2 \times \left(\frac{1-0.48^2}{1-NA^2}\right) \times \text{FOT114 Rated Output Power}$$

where

Dia = cable fiber core Dia (μm) up to 375 maximum.

NA = effective cable NA up to 0.66 maximum (effective NA depends on cable length, decreasing with increased length to a "steady state" value).

Coupling into graded index fiber results in additional 3dB loss. See Typical Performance Curves for Launched Output Power versus Core Diameter and versus Numerical Aperture. For receiver details see the data sheet on the Burr-Brown FOR110.

The Burr-Brown 3712R and 3713R receivers can also be used, however, the fiber optic connectors are different.

TABLE II. FOT114/FOR110 Compatible Cable Manufacturers.

American Fiber Optic Corp.
1196 East Willow St.
Signal Hill, CA 90000

Belden Corporation
Fiber Optics
2000 S. Bavaria Ave.
Geneva, IL 60134
312 232-8900

Ensign-Bickford Industries, Inc.
660 Hopmeadow St.
Simsbury, CT 06070
203 658-4411

Maxlight Fiber Optic Div.
Raychem Corp. of Arizona
3035 N. 33rd Drive
Phoenix, AZ 85017
602 269-8387

Nissho-Iwai American Corp.
Broadway Plaza
Suite 1900
700 South Flower Street
Los Angeles, CA 90017
213 688-0684

Quartz Products Corporation
688 Somerset St.
P.O. Box 1347
Plainfield, NJ 07061
201 757-4545

Siecor Optical Cables, Inc.
P.O. Box 489
Hickory, NC 28601
704 324-3801

Telecommunication Products
Corning Glass Works
Corning, NY 14831
607 974-4411

Valtec
99 Hartwell St.
West Boylston, MA 01583
617 835-6082

GE Optical Fibers
Church Road
Leyton, London E107JH

Hytran Products
Pilkington P.E. Limited
Glascoed Rd. St. Asaph
Clwyd LL 17 OLL, UK
0745-583301

N.V. Phillips
Gloeilampenfabrieken
Main Supply Group Glass
Industry Group Optics
5600 MD Eindhoven, Netherlands
040-783295/783212

TYPICAL APPLICATIONS

The FOT114/FOR110 Fiber Optic Data Link solves such data transmission problems as cross talk, ringing, and echos. Electromagnetic interference (EMI) is avoided when using a fiber optic data link in high noise environments.

Lightning damage to cables and connecting equipment can be eliminated where fiber optic cables replace metallic conductors. In refineries and chemical plants which have explosive atmospheres, sparks from shorted electrical cables are eliminated by the fiber optic cable - an intrinsic safety feature. The unique features of the FOT114 allow it to be used directly with transducers requiring high sensitivity and linearity. Also, an inexpensive analog-to-digital converter can readily be constructed. Figures 8 thru 11 illustrate the use of the FOT114 transmitter and FOR110 receiver.

One major application of the FOT114 is a Remote Transducer Readout, Figure 8. This arrangement utilizes the key features of sensitivity and linearity. The transducer can be connected directly to the FOT114 input eliminating the requirement for an external precision instrumentation amplifier. Recovery of the analog signal can be achieved by a frequency-to-voltage converter such as the VFC42. A digital display can easily be produced by counting the TTL pulses from the output of the FOR110. In Figure 10, voice can be amplitude modulated and a sensor can be frequency modulated over the same cable. Also, two-channel multiplexing is possible as shown in Figure 11.

TABLE III. Calculated Link Lengths for Selected Cables (FOT114 to FOR110)[1].

TRANSMITTER	CABLE TYPE	FIBER CORE DIAMETER μm	FIBER EFFECTIVE[2] NA	FIBER LOSS[2] dB/km		LINK LENGTH m	
				TYP	MAX	MINIMUM[3]	TYPICAL
FOT114KG Red LED	All Plastic[4]	368	0.42	260	270	113	141
	Glass/Glass[5]	200	0.38	80	85	284	381
	Plastic Clad Silica[6]	200	0.34	12	15	1540	2450
	Telecom Silica[7]	50	0.20			Not recommended	
	Telecom Silica[8]	100	0.28	9	12	1143	2225
	Light Duty Plactic[9]	400	0.5	380	720	43	100
FOT114KG-IR IR LED	All Plastic[4]	368	0.42	800	850	47	58
	Glass/Glass[5]	200	0.35	35	45	742	1134
	Plastic Clad Silica[10]	200	0.33	15	20	1640	2607
	Telecom Silica[7]	50	0.20	2	2.5	5241	9702
	Telecom Silica[8]	100	0.27	4.5	7	3340	6596

NOTES:
(1) At +25°C, for temperature relationship see Typical Performance Curves. Lengths can be determined on the basis of power launched, losses, and receiver sensitivity for 10^{-6} bit error rate. (2) Best estimate of NA at this length. (3) Worst case max fiber loss = FOT114 min output power, FOR110 worst-case sensitivity. (4) Dupont PIFAX PIR-140. (5) Siecor 155 Super Fat. (6) Maxlight MSC200A. (7) Corning 2510F. (8) Corning SDF. (9) Burr-Brown OCA201-XX terminated cable assembly. (10) Maxlight MSC200B.

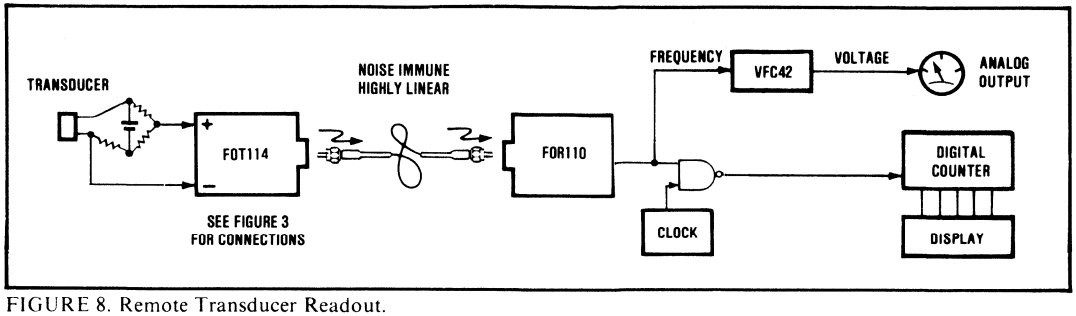


FIGURE 8. Remote Transducer Readout.

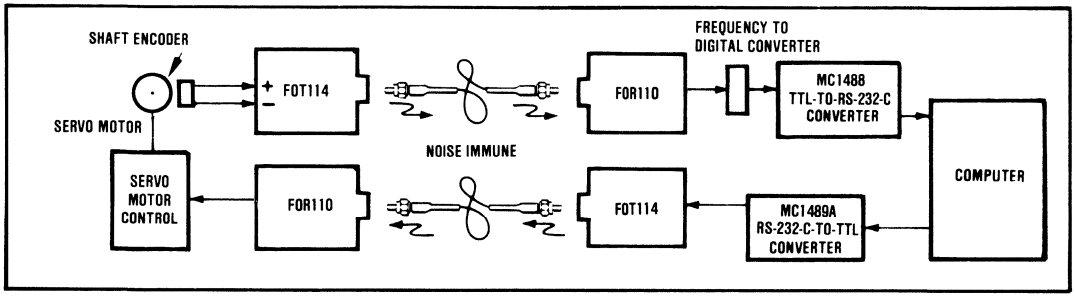


FIGURE 9. Monitor and Control System for a Servo Motor.

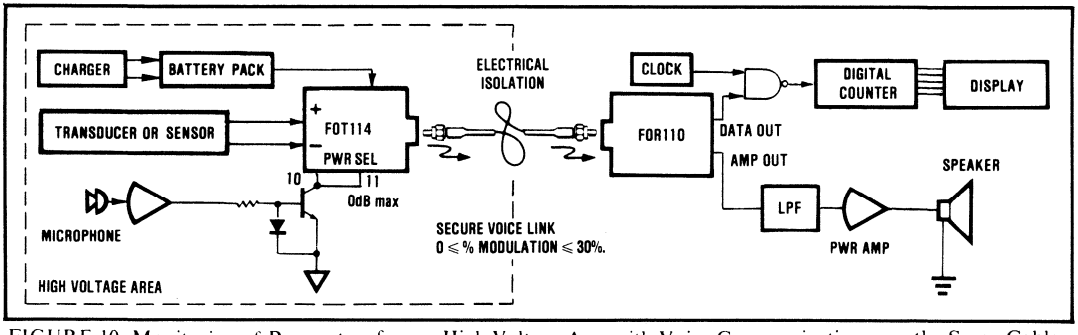


FIGURE 10. Monitoring of Parameters from a High Voltage Area with Voice Communication over the Same Cable.

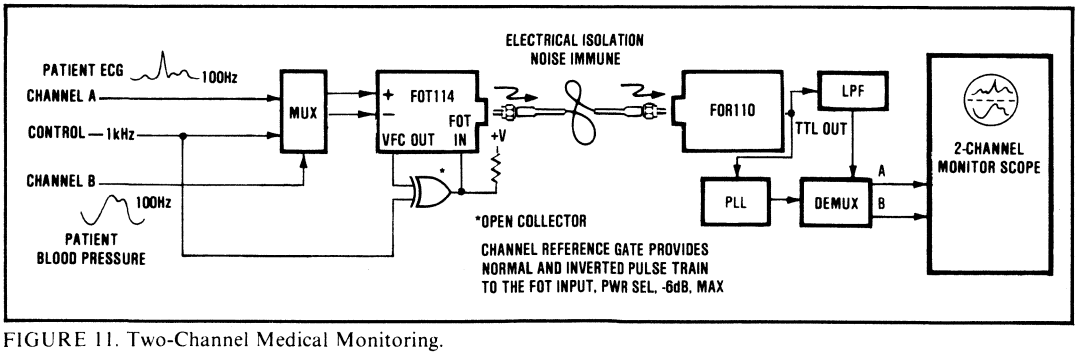


FIGURE 11. Two-Channel Medical Monitoring.

DESIGN EXAMPLE FOR THE FOT114KG

The following example demonstrates the procedure used to set up the FOT114KG for a low level analog input to parallel digital output application. The link requirements used are arbitrary, but chosen to show an analysis that should apply to most applications. Refer to Figure 14 for a diagram of the basic link connection.

LINK REQUIREMENTS

Type of Input	Strain gauge in bridge configuration
Input Voltage Range	±20mV
Required Resolution	0.024% FSR
Required Conversion Time	200msec
Method of Conversion	Gated counter
Link Length	500 meters
Cable Type	Corning SDF
Receiver Used	Burr-Brown FOR110KG
Output Format	12-bit parallel

PROCEDURE

Set the gain of the IA to take advantage of the full input range of the VFC which is 10V.

1. The input ranges over 40mV; therefore the IA gain should be,

$$\text{Gain} = \frac{V_O}{V_{IN}} = \frac{10}{0.04} = 250 \text{ V/V}$$

2. The gain setting resistor is given by,

$$G = 1 + \frac{40k}{R_G} \quad \text{or} \quad R_G = \frac{40k}{G - 1}$$

$$\text{therefore, } R_G = \frac{40k}{250 - 1} = 160.64\Omega$$

3. Select the closest standard value. A 162Ω 1% metal film resistor will provide good temperature stability.

Configure the buffer to level shift the signal and provide a unipolar input to the VFC.

1. This is necessary as the VFC will accept only positive inputs. Note that if the input is unipolar, the buffer need not be used in which case its inputs should be grounded. Since the buffer is inverting, the signal inputs to the IA should be reversed so that the polarity of the buffer output will match the input.
2. The signal will be level-shifted by two times the voltage on the Buffer Reference pin. Therefore, to shift the signal by 5V, the reference voltage should be 2.5V
3. The reference may be derived from the +15V supply (if it is well regulated) using the circuit in Figure 12.

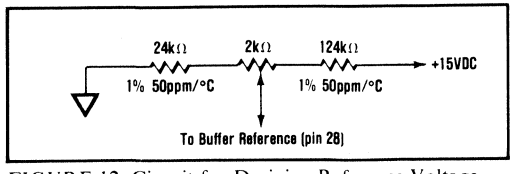


FIGURE 12. Circuit for Deriving Reference Voltage.

Set the full scale frequency of the VFC.

1. To realize a 12-bit converter with a 0.1sec gate time, a 40.96kHz full scale (FS) frequency is required. This could be established by either setting the FS output voltage of the IA to 4.096V and using the VFC section as is, or, by setting up the IA for a 10V full scale and configuring the VFC for a 40.96kHz output at 10V in. The latter is more desirable because it provides lower noise and improved linearity. Referring to the Linearity Error vs. Full Scale Frequency typical performance curve, a 40.96kHz FS frequency will usually yield a nonlinearity of less than 0.01% FSR.
2. Select external capacitor C1 to increase the pulse width according to the equation,

$$C_1 = (33 \times 10^{-6}) / F_{MAX} - 3.3 \times 10^{-10} \text{ (farads)}$$
$$= (33 \times 10^{-6}) / 40.96 \times 10^3 \; 0 \; 3.3 \times 10^{-10}$$
$$= 476\text{pF}$$

Use the closest standard value. A 500pF silver mica will provide good temperature stability. Note that in applications when the FS frequency is to remain at 100kHz care should be taken to minimize the parasitic capacitance at pin 1.

3. Select the external integrating capacitor C_2 according to the equation:

$$C_2 = (10^{-4} \; f_{MAX}) - 1.0 \times 10^{-9} \text{ (farads)}$$
$$= 10^{-4} \; 40.96 \times 10^3 - 10^{-9}$$
$$= 1441\text{pF}$$

Use the next highest standard value. A 1500pF mylar or polycarbonate capacitor is a good choice. The temperature coefficient is not critical but the dielectric absorption is important.

4. Select the appropriate potentiometer value to allow sufficient range of VFC gain adjustment to null both the IA and VFC errors. The nominal internal input resistance is 40kΩ. If it is parallel with a 270kΩ fixed resistor and a 10kΩ potentiometer is added in series, the resultant range of adjustment will be ±13% which is usually sufficient.

Select the correct output power for the cable and receiver used.

1. The required launched power (P_L) is determined by the necessary input power for the receiver (P_{IN}) and the fiber loss (LM). The minimum sensitivity of the FOR110KG is 32nW and the attenuation (LA) of Corning SDF is 12dB/km, maximum. Note that data on several cable types is available in Table III. For a link length of 500 meters, the fiber loss is:

$$LM = LA \times \text{length (km)} = 12 \times 0.5 = 6.0\text{dB}$$

2. The required launched power may be determined from the equation:

$$LM = 10 \log (P_L / P_{IN}) \text{ or } P_L = \text{Pin } 10^{LM/10}$$
$$P_L = 32\text{nW } 10^{6.0/10} = 127.39\text{nW}$$

3. Because the FOT110KG is specified for a 200μm core fiber and NA of 0.48, the launched power must be modified when using other types of fibers by the following equation:

$$P_L = \left(\frac{\text{Dia}}{200\mu\text{m}}\right)^2 \times \left(\frac{NA}{0.48}\right)^2 \times \left(\frac{1 - 0.48^2}{1 - NA^2}\right) \times \text{rated output power}$$

Corning SDF has a core diameter of 100μm and NA of 0.28. The launched power then becomes:

$$P_L = \left(\frac{100}{200}\right)^2 \times \left(\frac{0.28}{0.48}\right)^2 \times \left(\frac{1 - 0.48^2}{1 - 0.28^2}\right) \times \text{rated output power}$$

$$P_L = 0.071 \times \text{rated output power}$$

The actual output power required is found to be,

$$\text{Required output power for the 500 meter link} = \frac{P_L}{0.071} = \frac{127.39\text{nW}}{0.071} = 1.79\mu\text{W}$$

4. Referring to Table I (Optical Output Power vs Current) the closest output power greater than 1.79μW is 2.8μW which is typical for the -9dB setting. Additional loss such as those due to splices, intermediate connectors, and temperature should also be considered. Once the link is set up, the signal may be monitored at the Amplifier Output pin of the FOR110KG to insure that the signal level is sufficient. Note that higher output power may be used as long as the receiver input does not become saturated. Generally, it is considered beneficial to minimize output power to reduce power dissipation and supply requirements as well as extend LED lifetime.

Set the proper gate time for the digital counter to satisfy conversion time and resolution requirements.

A 5Hz square wave provides a gate time of 100msec and an additional 100msec to latch and reset the counter. The conversion time is 200msec and resolution is given by,

$$\text{Resolution} = \frac{100}{\text{Gate Time x FS Frequency}} = \frac{100}{0.1 \times 40960} = 0.024\%\ \text{FS}$$

This resolution corresponds to 12 bits. The typical linearity error of the FOT114, 0.01% at 40.96kHz FS, provides an overall accuracy of $\pm$1/2LSB. Note that the gate signal and FOR110KG output are asynchronous, resulting in an inherent uncertainty of +1LSB. 1LSB corresponds to 9.77μV at the input.

Calibrate using the procedure in the Gain and Offset Adjustment section. Alternately apply a -19.961mV and +20mV input and adjust for a binary output of 4 and 4096 respectively. Figure 13 is a timing diagram.

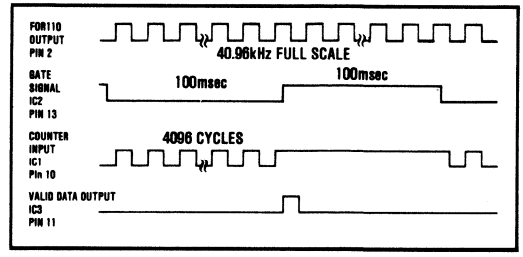


FIGURE 13. Timing Diagram.

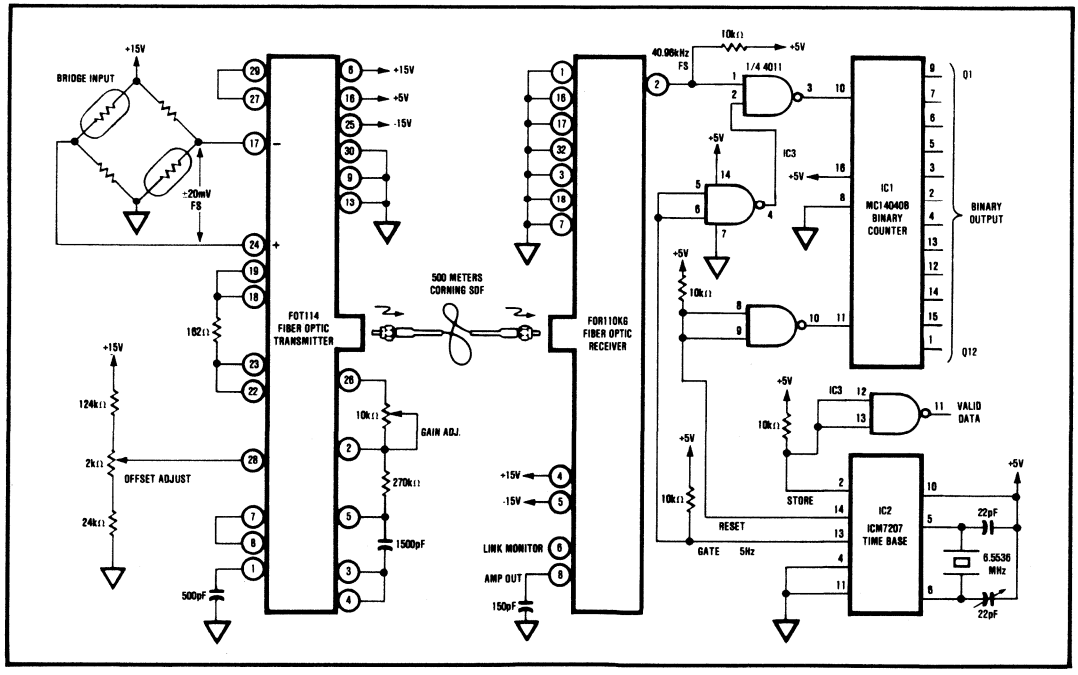


FIGURE 14. Complete System Schematic for FOT114KG - FOR110KG Design Example.

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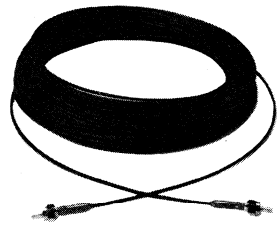


OCA201

Step-Index
FIBER OPTIC CABLE ASSEMBLY

FEATURES

- FACTORY-INSTALLED CONNECTORS
- USER-SPECIFIED LENGTH
- IMMUNITY FROM EMI AND RFI
- NO RADIATED RF
- ELIMINATES GROUND LOOPS AND SHORT CIRCUITS
- ELIMINATES EXPLOSION AND FIRE HAZARD
- GUARANTEED COMPATIBILITY WITH BURR-BROWN "FOT" AND "FOR" SERIES TRANSMITTERS AND RECEIVERS

APPLICATIONS

- INDUSTRIAL/PROCESS CONTROL SYSTEMS ELECTRICALLY NOISY ENVIRONMENTS
- REMOTE INSTRUMENTATION SYSTEMS
- POWER PLANT CONTROL
- HIGH VOLTAGE OR ELECTROMAGNETIC FIELD RESEARCH
- FACTORY DATA COLLECTION
- SECURITY SYSTEMS
- INTRINSIC SAFETY
- MACHINE TOOL CONTROL

DESCRIPTION

The OCA201 is a factory-terminated fiber optic cable assembly. The connectors used on the OCA201 are industry standard SMA type compatible with all Burr-Brown "FOT/FOR" series fiber optic products. The cable used is an all-plastic step-index variety suitable for use in the visible red spectrum. Due to high attenuation of plastic core fiber in the IR spectrum, the OCA201 is not recommended for use with IR transmitters.

Although this cable assembly is intended primarily for demonstration and educational use, it is suitable for many short-haul, light duty applications. Because the cable is not reinforced, tensile loads must be limited.

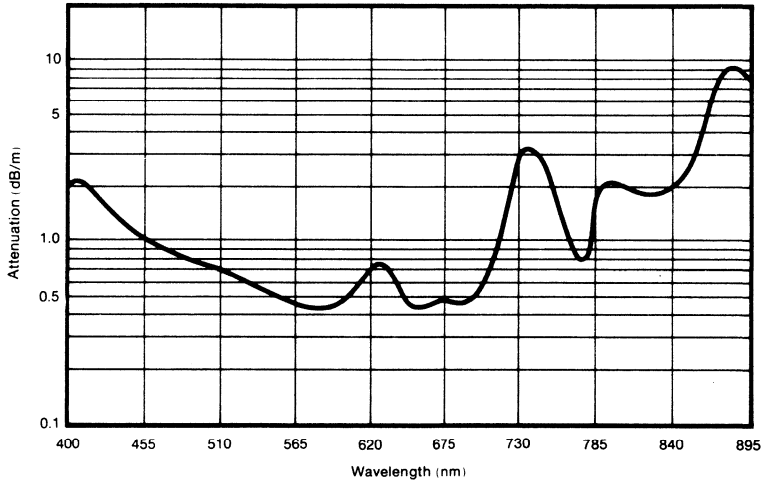
International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

At +25°C unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OPTICAL					
Attenuation	λ = 665nm	0.25		0.72	dB/m
Numerical Aperture	Material		0.5		
MECHANICAL					
Core Diameter			500		μm
Cable Diameter		0.83		2.4	mm
Cable Tensile					
Yield		2			KG
Bend Radius	Short Term	5			mm
Bend Radius	Long Term	25			mm
Operating Temperature	Tensile Force = 0			+70	°C
Operating Temperature	Bend = 0	-20			°C
Cable Weight				0.25	Gm/m
Connector Type	SMA				

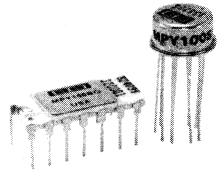
TYPICAL PERFORMANCE CURVE



ORDERING INFORMATION

To order, specify the cable part number (OCA201) and desired length to the nearest meter. Example for 10 meters: OCA201-10

BURR-BROWN®



MPY100

MULTIPLIER-DIVIDER

FEATURES

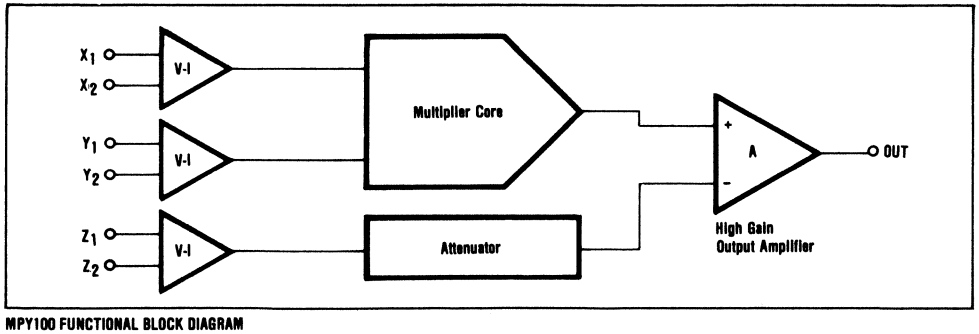
- LOW COST
- DIFFERENTIAL INPUT
- ACCURACY 100% TESTED AND GUARANTEED
- NO EXTERNAL TRIMMING REQUIRED
- LOW NOISE
  90μV, rms, 10Hz to 10kHz
- HIGHLY RELIABLE ONE-CHIP DESIGN
- DIP OR TO-100 TYPE PACKAGE
- WIDE TEMPERATURE OPERATION

APPLICATIONS

- MULTIPLICATION
- DIVISION
- SQUARING
- SQUARE ROOT
- LINEARIZATION
- POWER COMPUTATION
- ANALOG SIGNAL PROCESSING
- ALGEBRAIC COMPUTATION
- TRUE RMS-TO-DC CONVERSION

DESCRIPTION

The MPY100 multiplier-divider is a low cost precision device designed for general purpose application. In addition to four-quadrant multiplication, it also performs analog square root and division without the bother of external amplifiers or potentiometers. Laser-trimmed one-chip design offers the most in highly reliable operation with guaranteed accuracies. Because of the internal reference and pretrimmed accuracies the MPY100 does not have the restrictions of other low cost multipliers. It is available in both TO-100 and DIP ceramic packages.



MPY100 FUNCTIONAL BLOCK DIAGRAM

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

Specifications at T_A = +25°C and $\pm V_S$ = 15VDC unless otherwise noted.

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
MULTIPLIER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X, Y ≤ 10V										
Initial	T_A = +25°C			±2.0			±1.0/0.5			±0.5	% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.017	±0.05		±0.008/0.008	±0.02/0.02				% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.025	±0.05	% FSR/°C
vs. Supply(1)			±0.05			*/*			*		% FSR/%
Individual Errors											
Output Offset											
Initial	T_A = +25°C		±50	±100		±10/7	±50/25		±7	±50mV	mV
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.7	±2.0		±0.7/0.3	±2.0/±0.7				mV/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.3	±0.7	mV/°C
vs. Supply(1)			±0.25			*/*			*		mV/%
Scale Factor Error											
Initial	T_A = +25°C		±0.12			*/*			*		% FSR
vs. Temperature	-25°C ≤ T_A ≤ +85°C		±0.008			*/*					% FSR/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								±0.008		% FSR/°C
vs. Supply(1)			±0.05			*/*			*		% FSR/%
Nonlinearity											
X Input	X = 20V, p-p; Y = ±10VDC		±0.08			*/*			*		% FSR
Y Input	Y = 20V, p-p; X = ±10VDC		±0.08			*/*			*		% FSR
Feedthrough	f = 50Hz										
X Input	X = 20V, p-p; Y = 0		100			30/30			30		mV, p-p
Y Input	Y = 20V, p-p; X = 0		6			*/*			*		mV, p-p
vs. Temperature	-25°C ≤ T_A ≤ +85°C		0.1			*/*					mV, p-p/°C
vs. Temperature	-55°C ≤ T_A ≤ +125°C								0.1		mV, p-p/°C
vs. Supply(1)			0.15			*/*			*		mV, p-p/%
DIVIDER PERFORMANCE											
Transfer Function	$X_1 > X_2$		$\frac{10(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$			*/*			*		
Total Error with external adjustments	X = 10V										
	-10V ≤ Z ≤+10V		±1.5			±0.75/0.35			±0.35		% FSR
	X = 1V										
	-1V ≤ Z ≤ +1V		±4.0			±2.0/1.0			±1.0		% FSR
	+0.2V ≤ X ≤ +10V										
	-10V ≤ Z ≤ +10V		±5.0			±2.5/1.0			±1.0		% FSR
SQUARER PERFORMANCE											
Transfer Function			$\frac{(X_1 - X_2)^2}{10} + Z_2$			*/*			*		
Total Error	-10V ≤ X ≤ +10V		±1.2			±0.6/0.3			±0.3		% FSR
SQUARE-ROOTER PERFORMANCE											
Transfer Function	$Z_1 < Z_2$		$+\sqrt{10(Z_2 - Z_1)} + X_2$			*/*			*		
Total Error	1V ≤ Z ≤ 10V		±2			±1/0.5			±0.5		% FSR
AC PERFORMANCE											
Small-Signal Bandwidth			550			*/*			*		kHz
1% Amplitude Error	Small-Signal		70			*/*			*		kHz
1% 0.57° Vector Error	Small-Signal		5			*/*			*		kHz
Full Power Bandwidth	$\|V_O\|$ = 10V, R_L = 2kΩ		320			*/*			*		kHz
Slew Rate	$\|V_O\|$ = 10V, R_L = 2kΩ		20			*/*			*		V/μsec
Settling Time	ε = ±1%, ΔV_O = 20V		2			*/*			*		μsec
Overload Recovery	50% Output Overload		0.2			*/*			*		μsec
INPUT CHARACTERISTICS											
Input Voltage Range											
Rated Operation		±10			*/*			*			V
Absolute Maximum				±V_{CC}			*/*			*	V
Input Resistance	X, Y, Z(2)		10			*/*			*		MΩ
Input Bias Current	X, Y, Z		1.4			*/*			*		μA
OUTPUT CHARACTERISTICS											
Rated Output											
Voltage	I_O = ±5mA	±10			*/*			*			V
Current	V_O = ±10V	±5			*/*			*			mA
Output Resistance	f = DC		1.5			*/*			*		Ω
OUTPUT NOISE VOLTAGE	X = Y = 0										
f_O = 1Hz			6.2			*/*			*		μV/√Hz
f_O = 1kHz			0.6			*/*			*		μV/√Hz
1/f Corner Frequency			110			*/*			*		Hz
f_B = 5Hz to 10kHz			60			*/*			*		μV, rms
f_B = 5Hz to 5MHz			1.3			*/*			*		mV, rms
POWER SUPPLY REQUIREMENTS											
Rated Voltage			±15			*/*			*		VDC
Operating Range	Derated Performance	±8.5		±20	*/*		*/*	*		*	VDC
Quiescent Current			±5.5			*/*			*/*		mA

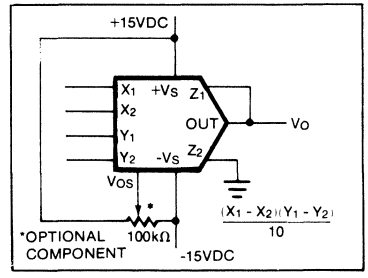
ELECTRICAL SPECIFICATIONS (CONT)

MODEL		MPY100A			MPY100B/C			MPY100S			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TEMPERATURE RANGE (Ambient)											
Specification	Derated Performance	-25		+85	*/*		*/*	-55		+125	°C
Operating Range		-55		+125	*/*		*/*	*		*	°C
Storage		-65		+150	*/*		*/*	*		*	°C

NOTES:
1. Includes effects of recommended null pots.
2. Z_2 input resistance is 10MΩ, typical, with V_{OS} pin open. If V_{OS} pin is grounded or used for optional offset adjustment, the Z_2 input resistance may be as low as 25kΩ.

*Same as MPY100A specification. */* means B/C grades same as MPY100A specification.

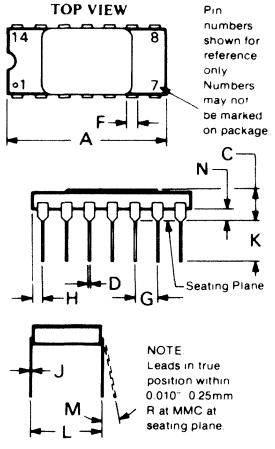
CONNECTION DIAGRAM



MECHANICAL

CERAMIC DUAL-IN-LINE PACKAGE

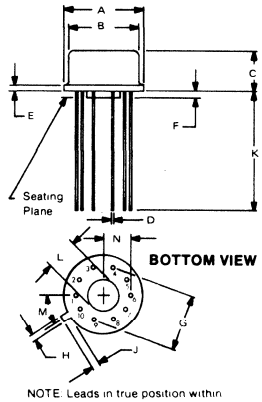
Order Number:
MPY100AG, MPY100BG
MPY100CG, MPY100SG



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

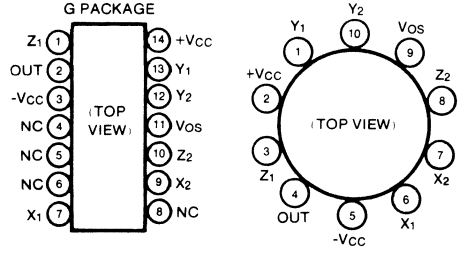
METAL CAN PACKAGE

Order Number:
MPY100AM, MPY100BM
MPY100CM, MPY100SM



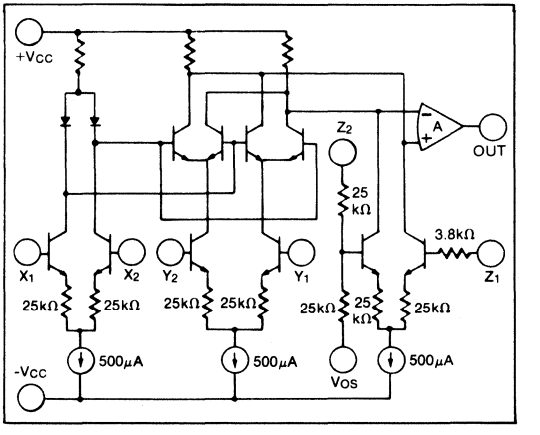
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

PIN CONFIGURATION



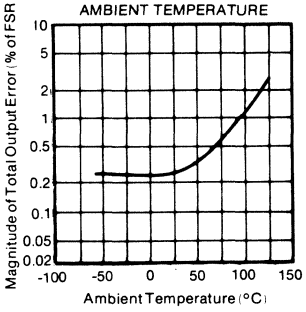
NOTES:
1. V_{OS} adjustment optional not normally recommended. V_{OS} pin may be left open or grounded.
2. All unused input pins should be grounded.

SIMPLIFIED SCHEMATIC

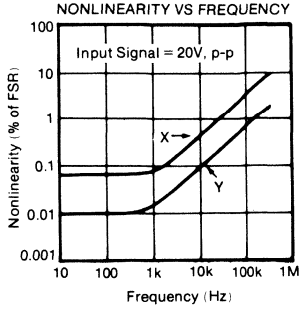


TYPICAL PERFORMANCE CURVES

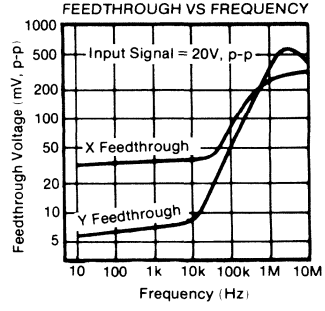
TOTAL ERROR VS AMBIENT TEMPERATURE



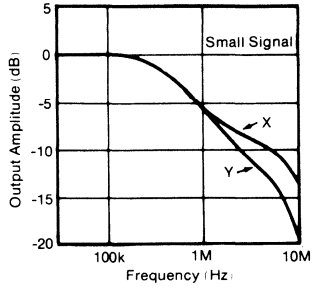
NONLINEARITY VS FREQUENCY



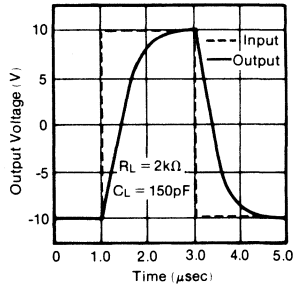
FEEDTHROUGH VS FREQUENCY



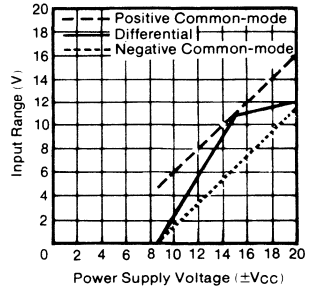
OUTPUT AMPLITUDE VS FREQUENCY



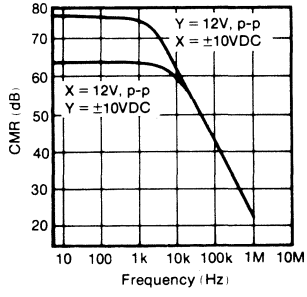
LARGE SIGNAL RESPONSE



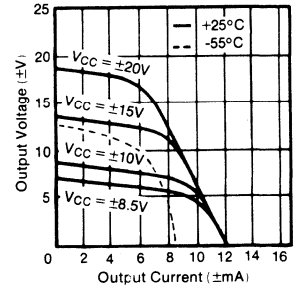
INPUT VOLTAGE FOR LINEAR RESPONSE



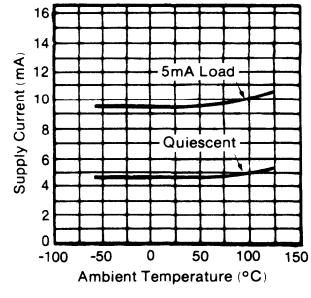
COMMON-MODE REJECTION VS FREQUENCY



OUTPUT VOLTAGE VS OUTPUT CURRENT



SUPPLY CURRENT VS AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM RATINGS

Supply	±20VDC
Internal Power Dissipation(1)	500mW
Differential Input Voltage(2)	±40VDC
Input Voltage Range(2)	±20VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short-circuit Duration(3)	Continuous
Junction Temperature	+150°C

NOTES:
1. Package must be derated on θ_{JC} = 15°C/W and θ_{JA} = 165°C/W for the metal package and θ_{JC} = 35°C/W and θ_{JA} = 220°C/W for the ceramic package.
2. For supply voltages less than ±20VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground only. Rating applies to +85°C ambient for the metal package and +65°C for the ceramic package.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The MPY100 is a variable transconductance multiplier consisting of three differential voltage-to-current converters, a multiplier core and an output differential amplifier as illustrated in Figure 1.

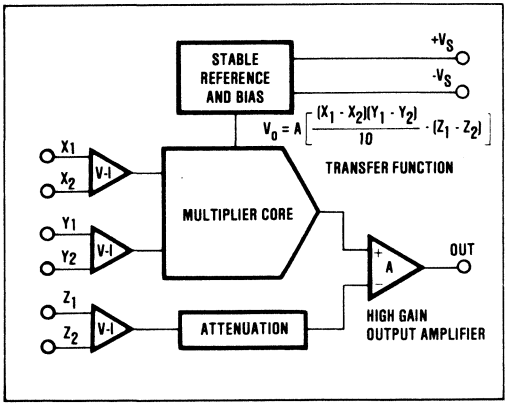


FIGURE 1. MPY100 Functional Block Diagram.

The basic principle of the transconductance multiplier can be demonstrated by the differential stage in Figure 2.

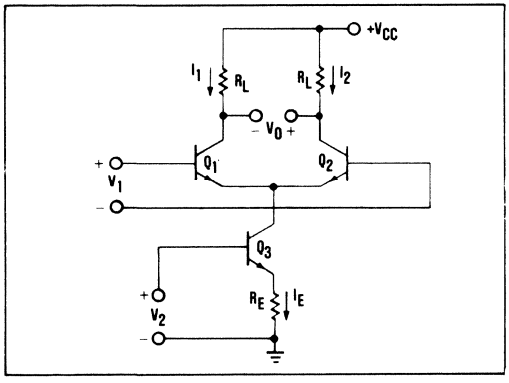


FIGURE 2. Basic Differential Stage as a Transconductance Multiplier.

For small values of the input voltage V_1 that are much smaller than V_T, the transistor's thermal voltage, the differential output voltage V_o is

$$V_o = g_m R_L V_1.$$

The transconductance g_m of the stage is given by:

$$g_m = I_E / V_T,$$

and is modulated by the voltage V_2 to give

$$g_m \approx V_2 / V_T R_E.$$

Substituting this into the original equation yields the overall transfer function

$$V_o = g_m R_L V_1 = V_1 V_2 (R_L / V_T R_E)$$

which shows the output voltage to be the product of the two input voltages, V_1 and V_2.

Variations in I_E due to V_2 cause a large common-mode voltage swing in the circuit. The errors associated with this common-mode voltage can be eliminated by using two differential stages in parallel and cross-coupling their outputs as shown in Figure 3.

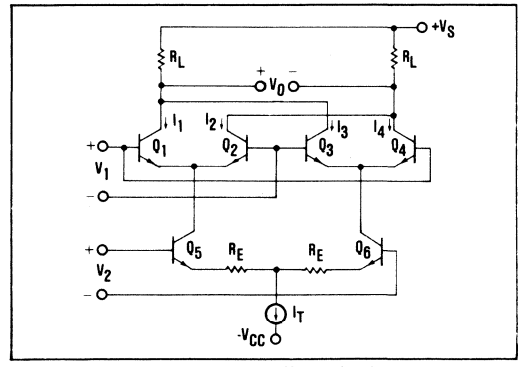


FIGURE 3. Cross-coupled Differential Stages as a Variable-transconductance Multiplier.

An analysis of the circuit in Figure 3 shows it to have the same overall transfer function as before:

$$V_o = V_1 V_2 (R_L / V_T R_E).$$

For input voltages larger than V_T the voltage-to-current transfer characteristics of the differential pair Q_1, Q_2 or Q_3 and Q_4 are no longer linear. Instead, their collector currents are related to the applied voltage V_1 as

$$\frac{I_1}{I_2} = \frac{I_3}{I_4} = e^{\frac{V_1}{V_T}}$$

The resultant nonlinearity can be overcome by developing V_1 logarithmically to exactly cancel the exponential relationship just derived. This is done by diodes D_1 and D_2 in Figure 4.

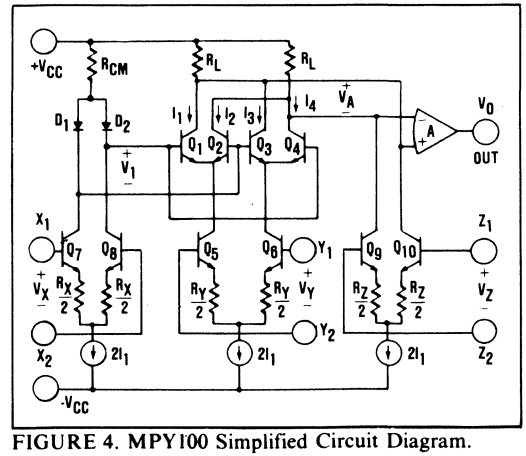


FIGURE 4. MPY100 Simplified Circuit Diagram.

The emitter degeneration resistors R_X and R_Y, in Figure 4, provide a linear conversion of the input voltages to differential current I_X and I_Y, where

$$I_X = V_X / R_X \text{ and } I_Y = V_Y / R_Y.$$

Analysis of Figure 4 shows the voltage V_A to be

$$V_A = (2R_L / I_1)(I_X I_Y).$$

Since I_X and I_Y are linearly related to the input voltages V_X and V_Y, V_A may also be written

$$V_A = KV_XV_Y$$

where K is a scale factor. In the MPY100, K is chosen to be 0.1.

The addition of the Z input alters the voltage V_A to

$$V_A = KV_XV_Y - V_Z.$$

Therefore, the output of the MPY100 is

$$V_o = A[KV_XV_Y - V_Z]$$

where A is the open-loop gain of the output amplifier. Writing this last equation in terms of the separate inputs to the MPY100 gives

$$V_o = A\left[\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} - (Z_1 - Z_2)\right],$$

the transfer function of the MPY100.

WIRING PRECAUTIONS

In order to prevent frequency instability due to lead inductance of the power supply lines, each power supply should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 1000pF ceramic capacitor from the $+V_{CC}$ and $-V_{CC}$ pins of the MPY100 to the power supply common. The connection of these capacitors should be as close to the MPY100 as practical.

CAPACITIVE LOADS

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root mode for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the MPY100's output.

DEFINITIONS

TOTAL ERROR (Accuracy)

Total error is the actual departure of the multiplier output voltage from the ideal product of its input voltages. It includes the sum of the effects of input and output DC offsets, gain error and nonlinearity.

OUTPUT OFFSET

Output offset is the output voltage when both inputs V_X and V_Y are zero volts.

SCALE FACTOR ERROR

Scale factor error is the difference between the actual scale factor and the ideal scale factor.

NONLINEARITY

Nonlinearity is the maximum deviation from a best straightline (curve fitting on input-output graph) expressed as a percent of peak-to-peak full scale output.

FEEDTHROUGH

Feedthrough is the signal at the output for any value of V_X or V_Y within the rated range, when the other input is zero.

SMALL SIGNAL BANDWIDTH

Small signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value for a nominal output amplitude of 10% of full scale.

1% AMPLITUDE ERROR

The 1% amplitude error is the frequency the output amplitude is in error by 1%, measured with an output amplitude of 10% of full scale.

1% VECTOR ERROR

The 1% vector error is the frequency at which a phase error of 0.01 radians (0.57°) occurs. This is the most sensitive measure of dynamic error of a multiplier.

TYPICAL APPLICATIONS

MULTIPLICATION

Figure 5 shows the basic connection for four-quadrant multiplication.

The MPY100 meets all of its specifications without trimming. Accuracy can, however, be improved by nulling the output offset voltage using the 100kΩ optional balance potentiometer shown in Figure 5.

AC feedthrough may be reduced to a minimum by applying an external voltage to the X or Y input as shown in Figure 6.

Z_2, the optional summing input, may be used to sum a voltage into the output of the MPY100. If not used, this

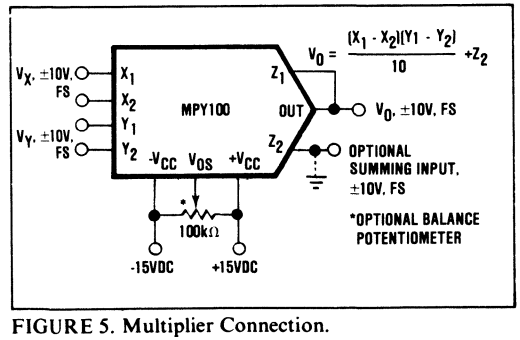


FIGURE 5. Multiplier Connection.

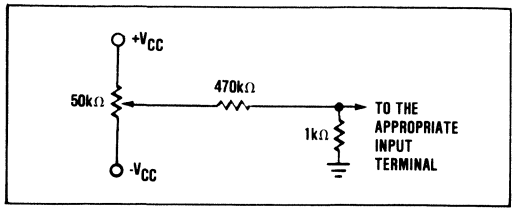


FIGURE 6. Optional Trimming Configuration.

terminal, as well as the X and Y input terminals, should be grounded. All inputs should be referenced to power supply common.

Figure 7 shows how to achieve a scale factor larger than the nominal 1/10. In this case, the scale factor is unity which makes the transfer function

$$V_o = KV_XV_Y = K(X_1 - X_2)(Y_1 - Y_2).$$

$$K = \frac{1 + (R_1/R_2)}{10}$$

$$0.1 \leq K \leq 1$$

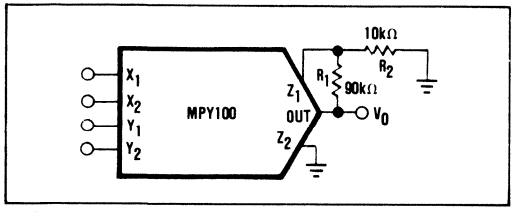


FIGURE 7. Connection For Unity Scale Factor.

This circuit has the disadvantage of increasing the output offset voltage by a factor of 10 which may require the use of the optional balance control as in Figure 1 for some applications. In addition, this connection reduces the small signal bandwidth to about 50kHz.

DIVISION

Figure 8 shows the basic connection for two-quadrant division. This configuration is a multiplier-inverted analog divider, i.e., a multiplier connected in the feedback loop of an operational amplifier. In the case of the MPY100 this operational amplifier is the output amplifier shown in Figure 1.

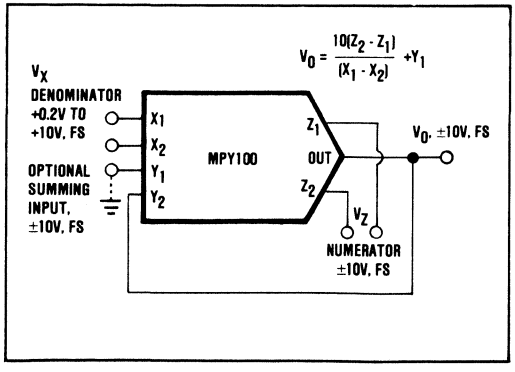


FIGURE 8. Divider Connection.

The divider error with a multiplier-inverted analog divider is approximately

$$\epsilon_{divider} = 10\ \epsilon_{multiplier}/(X_1 - X_2)$$

It is obvious from this error equation that divider error becomes excessively large for small values of $X_1 - X_2$. A 10-to-1 denominator range is usually the practical limit. If more accurate division is required over a wide range of denominator voltages, an externally generated voltage may be applied to the unused X-input (see Optional Trim Configuration). To trim, apply a ramp of +100mV to +1V at 100Hz to both X_1 and Z_1 if X_2 is used for offset adjustment, otherwise reverse the signal polarity, and adjust the trim voltage to minimize the variation in the output. An alternative to this procedure would be to use the Burr-Brown 4291, a precision log-antilog divider.

SQUARING

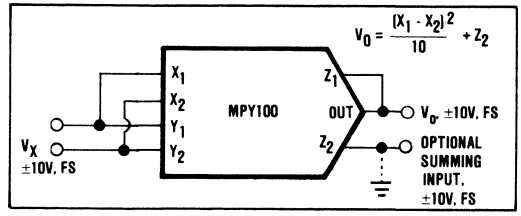


FIGURE 9. Squarer Connection.

SQUARE ROOT

Figure 10 shows the connection for taking the square root of the voltage V_Z. The diode prevents a latching condition which could occur if the input momentarily changed polarity. This latching condition is not a design flaw in the MPY100, but occurs when a multiplier is connected in the feedback loop of an operational amplifier to perform square root functions.

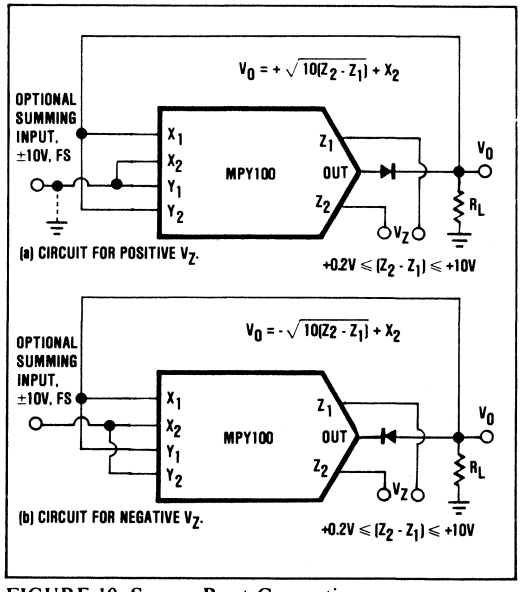


FIGURE 10. Square Root Connection.

The load resistance R_L must be in the range of $10k\Omega \leq R_L \leq 1M\Omega$. This resistance must be in the circuit as it provides the current necessary to operate the diode.

BRIDGE LINEARIZATION

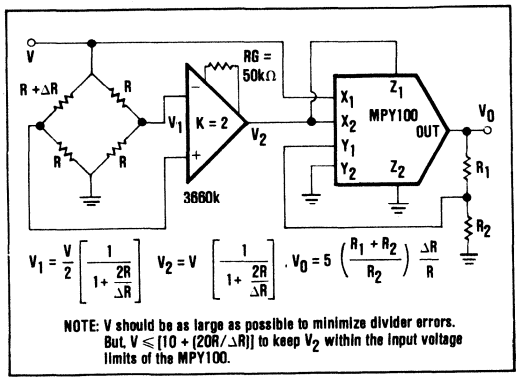


FIGURE 11. Bridge Linearization.

The use of the MPY100 to linearize the output from a bridge circuit makes the output V_o independent of the bridge supply voltage.

TRUE RMS-TO-DC CONVERSION

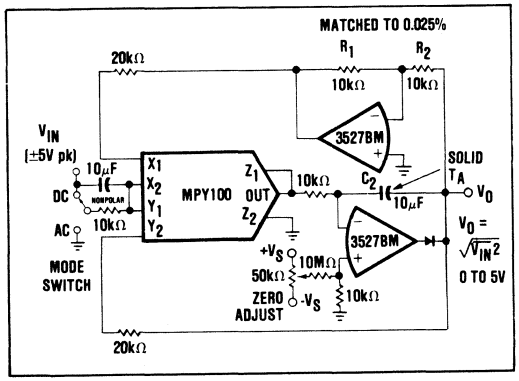


FIGURE 12. True RMS-to-DC Conversion.

The rms-to-DC conversion circuit of Figure 12 gives greater accuracy and bandwidth but with less dynamic range than most rms-to-DC converters.

PERCENTAGE COMPUTATION

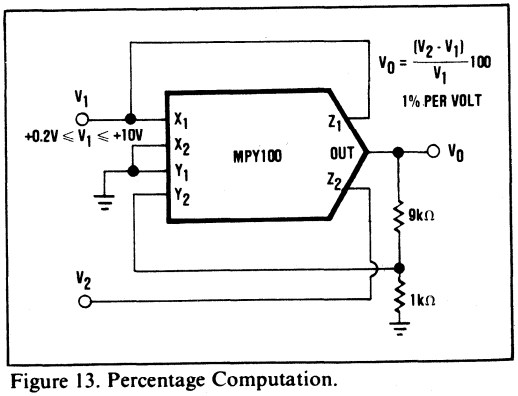


Figure 13. Percentage Computation.

The circuit of Figure 13 has a sensitivity of 1V/% and is capable of measuring 10% deviations. Wider deviation can be measured by decreasing the ratio of R_2/R_1.

SINE FUNCTION GENERATOR

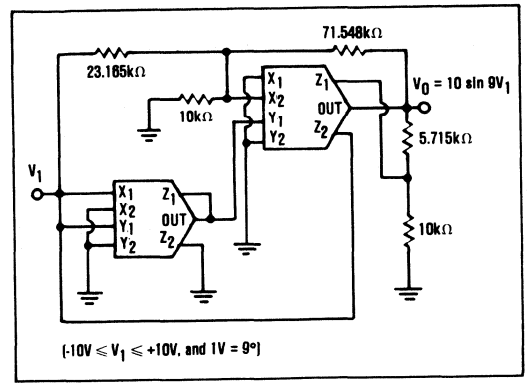


FIGURE 14. Sine Function Generator.

The circuit in Figure 14 uses implicit feedback to implement the following sine function approximation:

$$V_o = (1.5715V_1 - 0.004317V_1^3)(1 + 0.001398V_1^2)$$
$$= 10 \sin (9V_1).$$

SINGLE-PHASE POWER MEASUREMENT

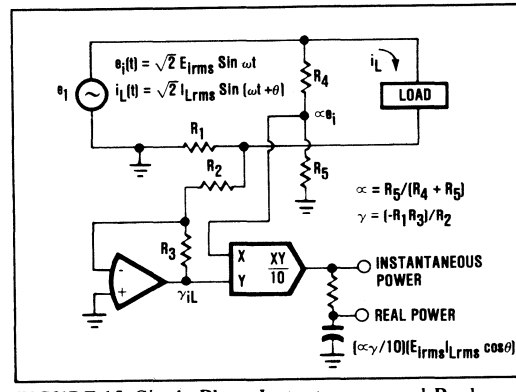


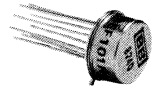
FIGURE 15. Single-Phase Instantaneous and Real Power Measurement.

MORE CIRCUITS

The theory and procedures for developing virtually any function generator or linearization circuit can be found in the Burr-Brown McGraw Hill book "FUNCTION CIRCUITS - Design and Applications."

BURR-BROWN®

REF101



Precision VOLTAGE REFERENCE

FEATURES

- +10.00V OUTPUT
- HIGH ACCURACY, ±0.005V
- VERY LOW DRIFT, 1ppm/°C max
- EXCELLENT STABILITY, 50ppm/1000hrs
- LOW NOISE, 6μV, p-p typ, 0.1Hz to 10Hz
- WIDE SUPPLY RANGE, up to 35V
- LOW QUIESCENT CURRENT, 6mA max
- USEFUL MATCHED RESISTOR PAIR INCLUDED

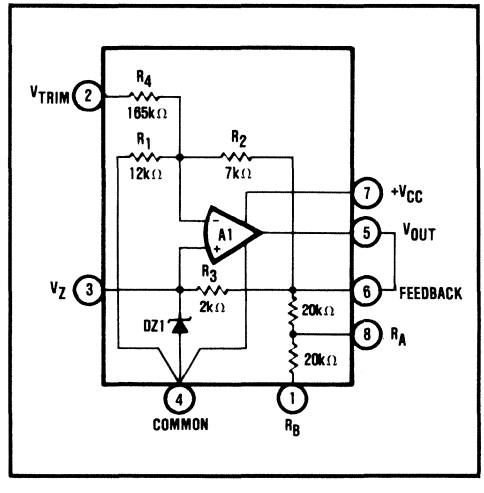
APPLICATIONS

- PRECISION CALIBRATED VOLTAGE STANDARD
- TRANSDUCER EXCITATION
- D/A AND A/D CONVERTER REFERENCE
- PRECISION CURRENT REFERENCE
- ACCURATE COMPARATOR THRESHOLD REFERENCE
- DIGITAL VOLTMETERS
- TEST EQUIPMENT

DESCRIPTION

The REF101 is a precision voltage reference which provides a +10.00V output. The drift is laser-trimmed to 1ppm/°C max (KM grade) over the full specification range. This is in contrast to some references which guarantee drift over a limited portion of their specification temperature range. The REF101 achieves its precision without a heater. This results in low quiescent current (4.5mA typ), fast warm-up (1msec to 0.1%), excellent stability (50ppm/1000hrs typ), and low noise (25μV, p-p max, 0.1Hz to 10Hz).

The output can be adjusted with minimal effect on drift or stability. Additionally, the REF101 contains a matched pair of user-accessible precision 20kΩ resistors which are useful in a variety of applications. Single supply operation over 13.5V to 35V supply range and excellent overall specifications make the REF101 an ideal choice for the most demanding applications such as precision system standards, D/A and A/D references, transducer excitation etc.



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SPECIFICATIONS

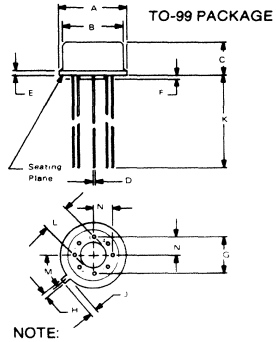
ELECTRICAL

At T_A = +25°C and +15VDC power supply unless otherwise noted.

PARAMETER	CONDITION	REF101JM/KM/RM/SM MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
Initial	T_A = +25°C	9.995	10.000	10.005	V
Trim Range(1)		-0.100		+0.250	V
vs Temperature(2)					
KM	0°C to +70°C			1	ppm/°C
JM	0°C to +70°C			2	ppm/°C
SM	-55°C to +125°C			3	ppm/°C
RM	-55°C to +125°C			6	ppm/°C
vs Supply (line regulation)	V_{CC} = 13.5 to 35V		0.001	0.002	%/V
vs Output Current					
(load regulation)	I_L = 0 to ±10mA		0.001	0.002	%/mA
vs Time	T_A = +25°C		50		ppm/1000 hrs
NOISE	0.1Hz to 10Hz		6	25	µV p-p
OUTPUT CURRENT	Source or Sink	±10			mA
INPUT VOLTAGE RANGE		13.5		35	V
QUIESCENT CURRENT	I_{OUT} = 0		4.5	6	mA
WARM-UP TIME	To 0.1%		10		µsec
UNCOMMITTED RESISTORS					
Resistance			20		kΩ
Match			±0.01	±0.05	%
TCR			50		ppm/°C
TCR Tracking			2		ppm/°C
TEMPERATURE RANGE					
Specification					
JM, KM		0		+70	°C
RM, SM		-55		+125	°C
Operating					
JM, KM		-25		+85	°C
RM, SM		-55		+125	°C
Storage		-65		+125	°C

NOTES:
1. Trimming the offset voltage will affect the drift slightly. See Installation and Operating Instructions for details.
2. The "box method" is used to specify output voltage drift vs temperature. See the Discussion of Performance section.

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers not marked on package.

Pin material and plating composition conform to Method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500	-	12.7	
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

WEIGHT: 1 gram
ORDER: REF101JM, REF101KM
REF101RM, REF101SM

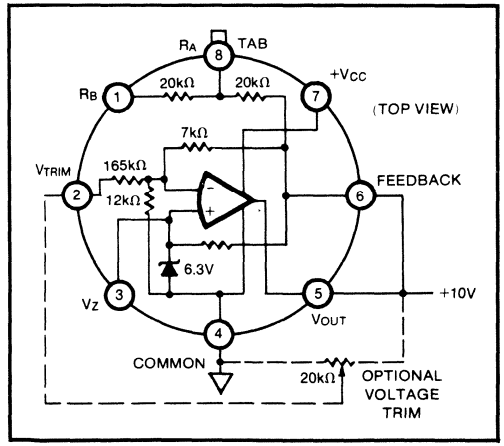
ORDERING INFORMATION

REF101 X M

Basic Model Number
Performance Grade Code
- J, K -25°C to +85°C
- R, S -55°C to +125°C

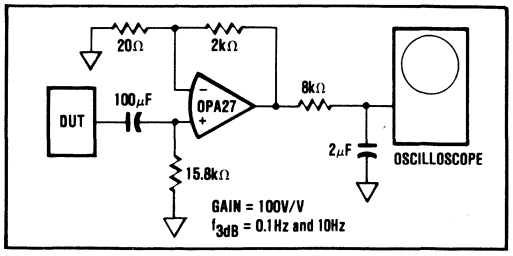
Package Code
- TO-99

PIN CONFIGURATION

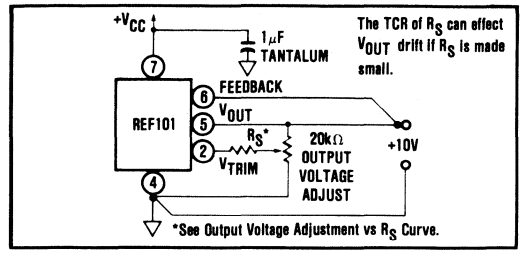


ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Power Dissipation at +25°C	200mW
Operating Temperature Range	
REF101JM/KM	-25°C to +85°C
REF101RM/SM	-55°C to +125°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (soldering, 10sec)	+300°C
Short-Circuit Protection at +25°C	
To Common or +15VDC	Continuous

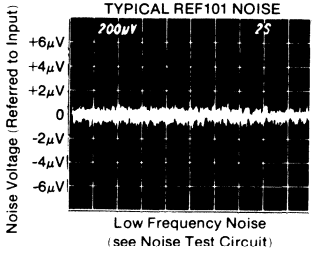


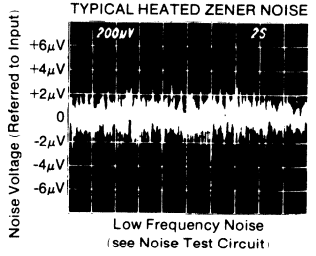
NOISE TEST CIRCUIT

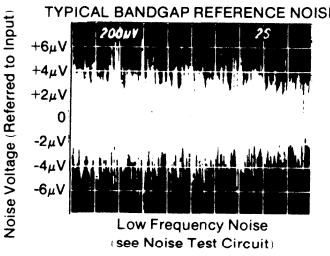


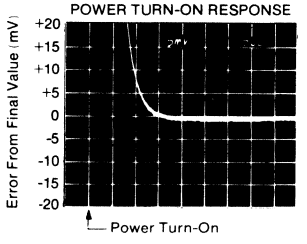
OPTIONAL OUTPUT VOLTAGE FINE ADJUSTMENT CIRCUIT.

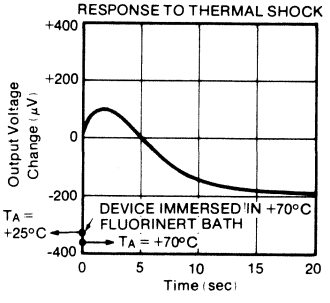
TYPICAL PERFORMANCE CURVES

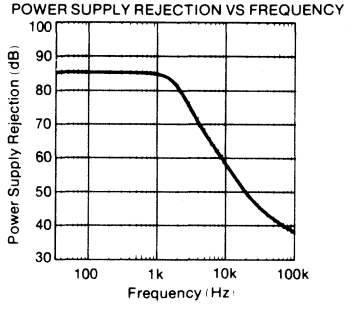


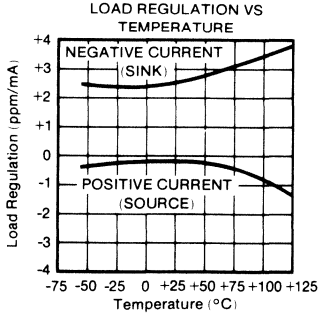


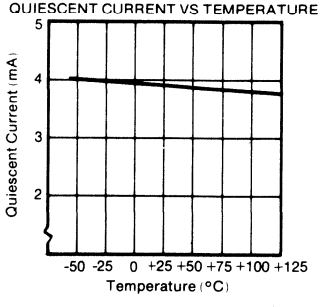


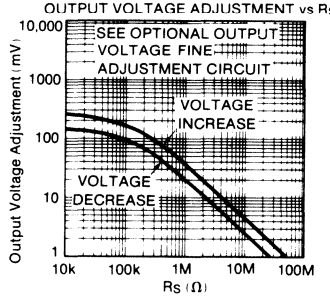


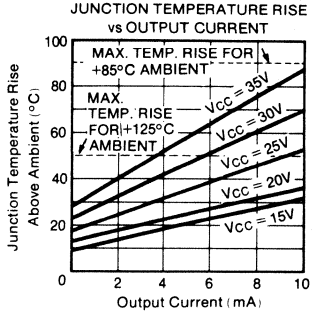












THEORY OF OPERATION

The following discussion refers to the diagram on the first page.

In operation, approximately 6.3V is applied to the noninverting input of op amp A_1 by zener diode DZ_1. This voltage is amplified by A_1 to produce the 10.00V output. The gain is determined by R_1 and R_2: $G = (R_1 + R_2)/R_1$. R_1 and R_2 are actively laser-trimmed to produce an exact 10.00V output. The zener operating current is derived from the regulated output voltage through R_3. This feedback arrangement provides closely regulated zener current. R_3 is actively laser-trimmed to set the zener current to a level which results in low drift at the output of A_1. The adjustment of output voltage and zener current is interactive and several iterations may be used to achieve the desired results. R_4 allows user-trimming of the output voltage by providing for a small external adjustment of amplifier gain. Since the TCR of R_4 closely matches the TCR of the gain setting resistors, the voltage trim has minimal effect on the drift of the reference.

DISCUSSION OF PERFORMANCE

The REF101 is designed for applications requiring a precision voltage reference where both the initial value at room temperature and the drift over temperature are of importance to the user. Two basic methods of specifying voltage reference drift versus temperature are in common usage in the industry — the "butterfly method" and the "box method". Neither of these methods is entirely satisfactory in cases where the drift versus temperature is relatively nonlinear as is the case with most voltage references. The REF101 is specified with the more commonly used box method. The "box" is formed by the high and low specification temperatures and a diagonal, the slope of which is equal to the maximum specified drift.

For the REF101 each J and K unit is tested at temperatures of 0°C, +25°C, +50°C, and +70°C and each R and S unit is tested at -55°C, -25°C, 0°C, +25°C, +50°C, +75°C, +100°C and +125°C. The minimum and maximum test voltages must meet this condition.

$$\left[\frac{(V_{OUT\ max} - V_{OUT\ min})/10V}{T_{high} - T_{low}}\right] \times 10^6 \leq \text{drift specification}$$

This assures the user that the variations of output voltage that occur as the temperature changes within the specification range T_{low} to T_{high} will be contained within a box whose diagonal has a slope equal to the maximum specified drift. Since the shape of the actual drift curve is not known, the vertical position of the box is not exactly known either. It is, however, bounded by $V_{Upper\ Bound}$ and $V_{Lower\ Bound}$ (see Figure 1).

Figure 1 uses the REF101KM as an example. It has a drift specification of 1ppm/°C maximum and a specification temperature range of 0°C to +70°C. The "box" height (V_1 to V_2) is 700μV and upper bound and lower bound voltages are a maximum of 700μV away from the voltage at +25°C.

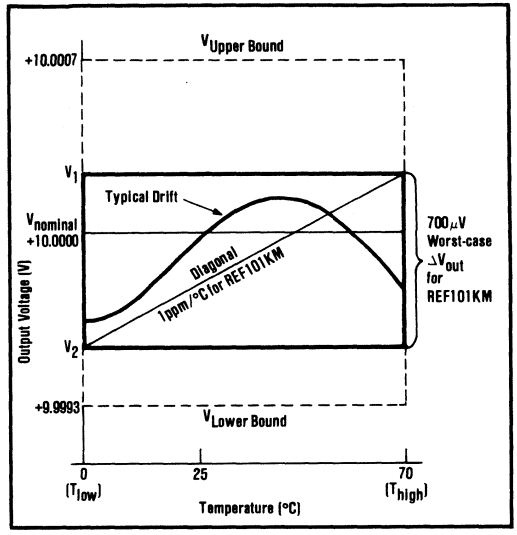
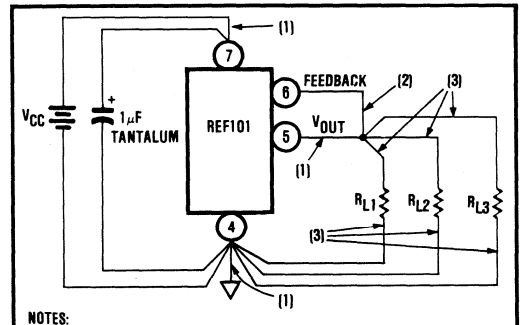


FIGURE 1. REF101KM Output Voltage Drift.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CIRCUIT CONNECTION

Figure 2 shows the proper connection of the REF101. To achieve the specified performance, pay careful attention to layout. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply. Commons should be connected as indicated being sure to minimize interconnection resistances.



NOTES:
1. Lead resistances here of up to a few ohms have negligible effect on performance.
2. A relatively constant current of approx. 2mA at 50ppm/°C flows in this lead. 1Ω in this lead would introduce about 2mV error (adjustable to zero) with about 0.1ppm/°C drift at the output.
3. A resistance of 0.1Ω in series with these leads will cause a 1mV error when the load current is at its maximum of 10mA. This results in a 0.01% error of 10V.

FIGURE 2. REF101 Basic Circuit Connection.

OPTIONAL OUTPUT VOLTAGE ADJUSTMENT

Optional output voltage adjustment circuits are shown in Figures 3 and 4. Trimming the output voltage will change the voltage drift by approximately 0.01ppm/°C per mV of trimmed voltage. In the circuit in Figure 3 any mismatch in TCR between the two sections of the potentiometer will also affect drift but the effect of the ΔTCR is reduced by a factor of 40 by the internal resistor divider. A high quality potentiometer, with good mechanical stability, such as a cermet, should be used. The circuit in Figure 3 has a range of approximately +250mV to -100mV. The circuit in Figure 4 has less range but provides higher resolution. The mismatch in TCR between R_S and the internal resistors can introduce some slight drift. This effect is minimized if R_S is kept significantly larger than the 165kΩ internal resistor. A TCR of 100ppm/°C is normally sufficient.

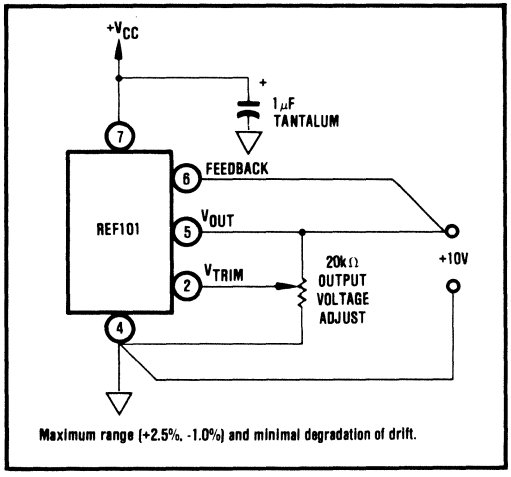


FIGURE 3. REF101 Optional Output Voltage Adjust.

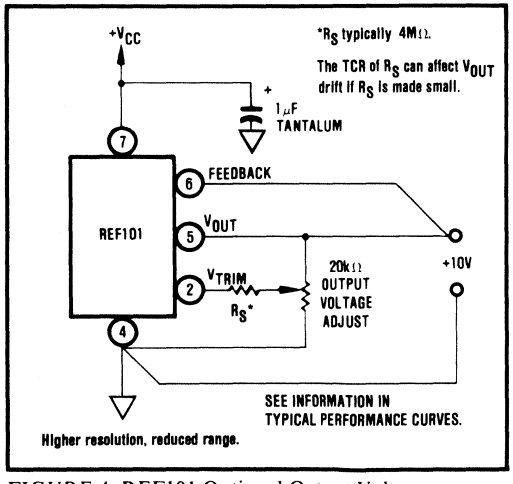


FIGURE 4. REF101 Optional Output Voltage Fine Adjust.

APPLICATION INFORMATION

High accuracy, extremely-low drift, and small size make the REF101 ideal for demanding instrumentation and system voltage reference applications. Since no heater is required, low power supply current designs are readily achievable. Also the REF101 has lower output noise and much faster warm-up times (1msec to 0.1%) than heated references, permitting high precision without extra power from additional supplies. It should be considered that operating any integrated circuit at an elevated temperature will reduce its MTTF.

A variety of application circuits are shown in Figures 5 through 19.

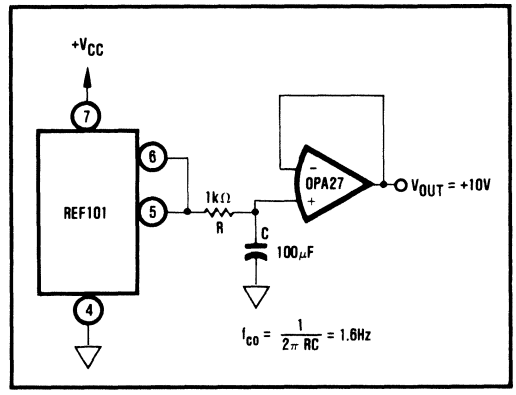


FIGURE 5. Precision Reference with Filtering.

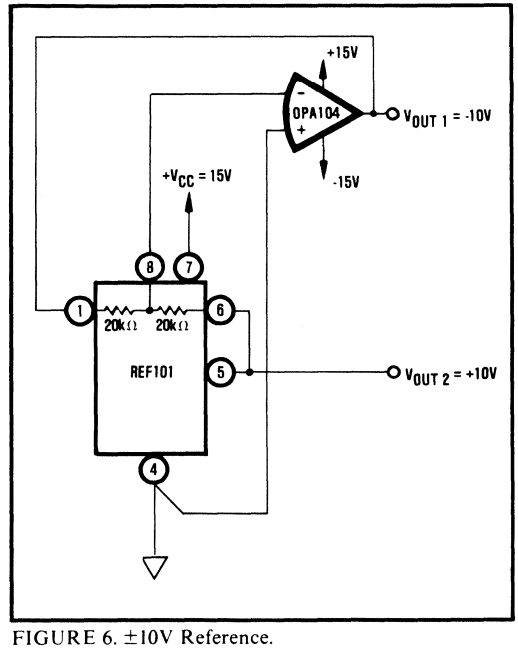


FIGURE 6. ±10V Reference.

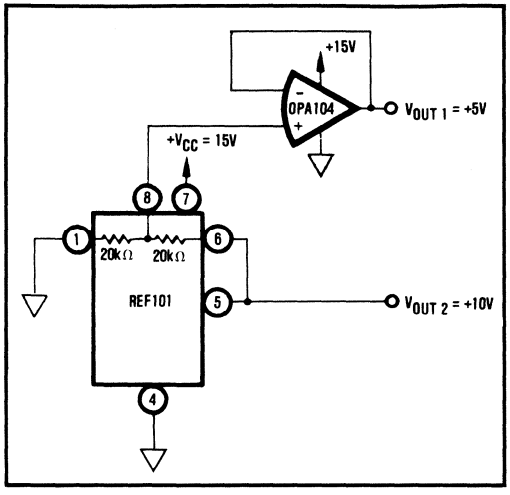


FIGURE 7. +10V and +5V Reference.

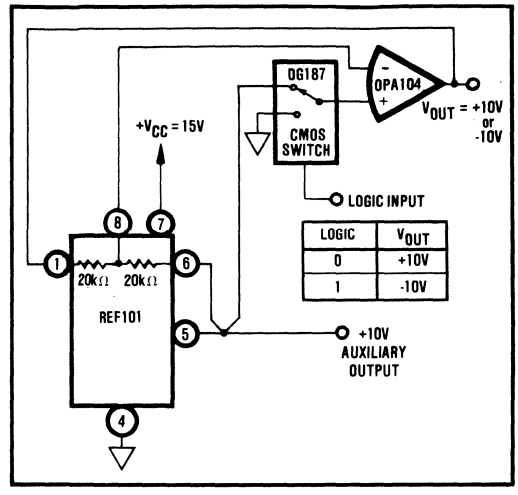


FIGURE 9. Digitally-Controlled Bipolar Precision Reference.

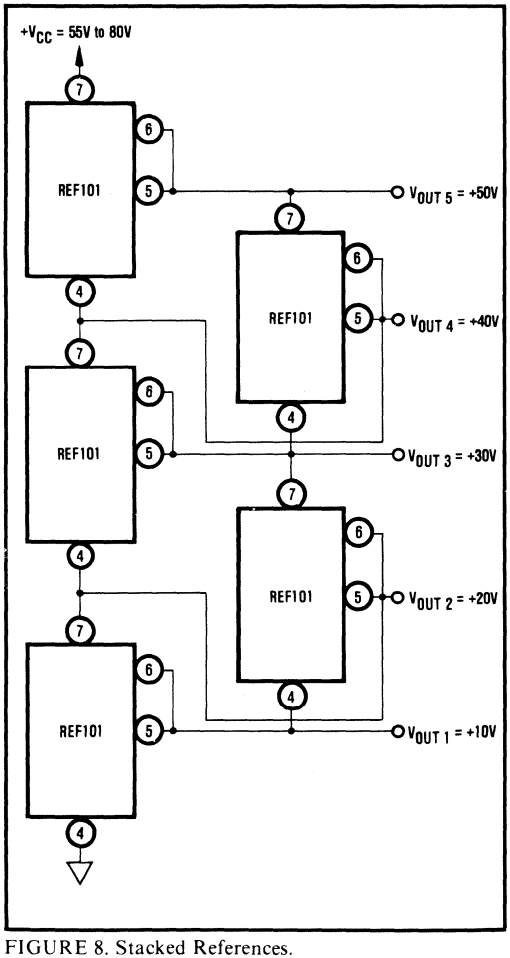


FIGURE 8. Stacked References.

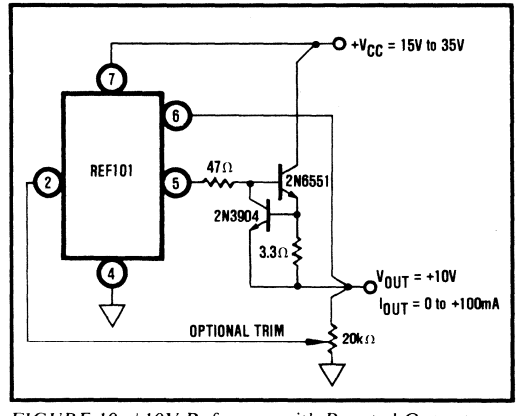


FIGURE 10. +10V Reference with Boosted Output Current to 100mA.

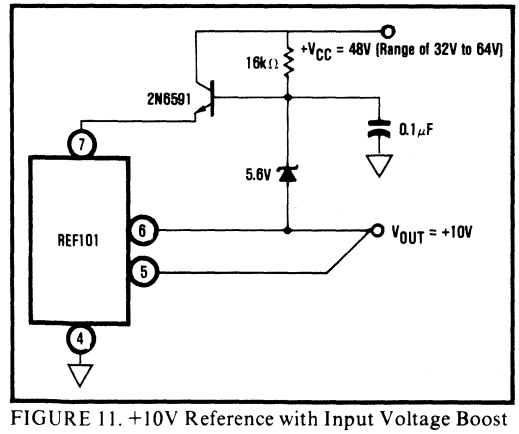


FIGURE 11. +10V Reference with Input Voltage Boost for 48V Operation.

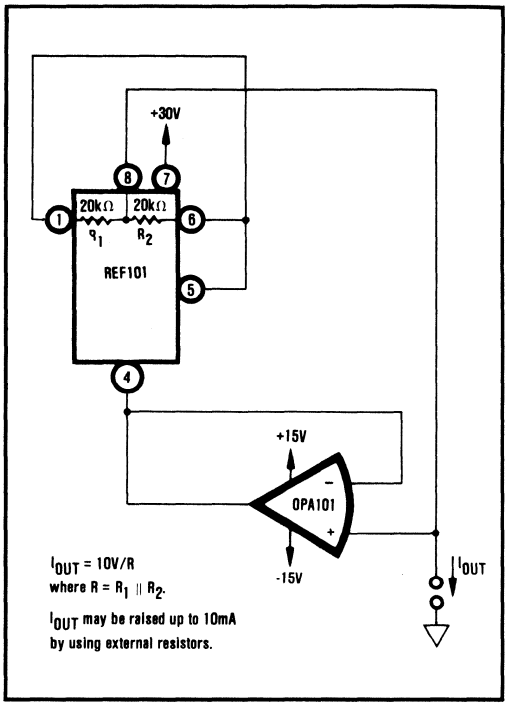


FIGURE 12. Positive Precision 1mA Current Source.

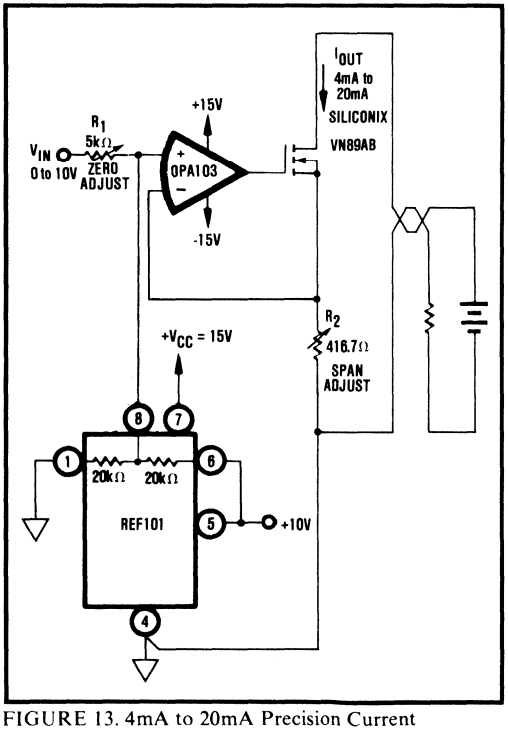


FIGURE 13. 4mA to 20mA Precision Current Transmitter.

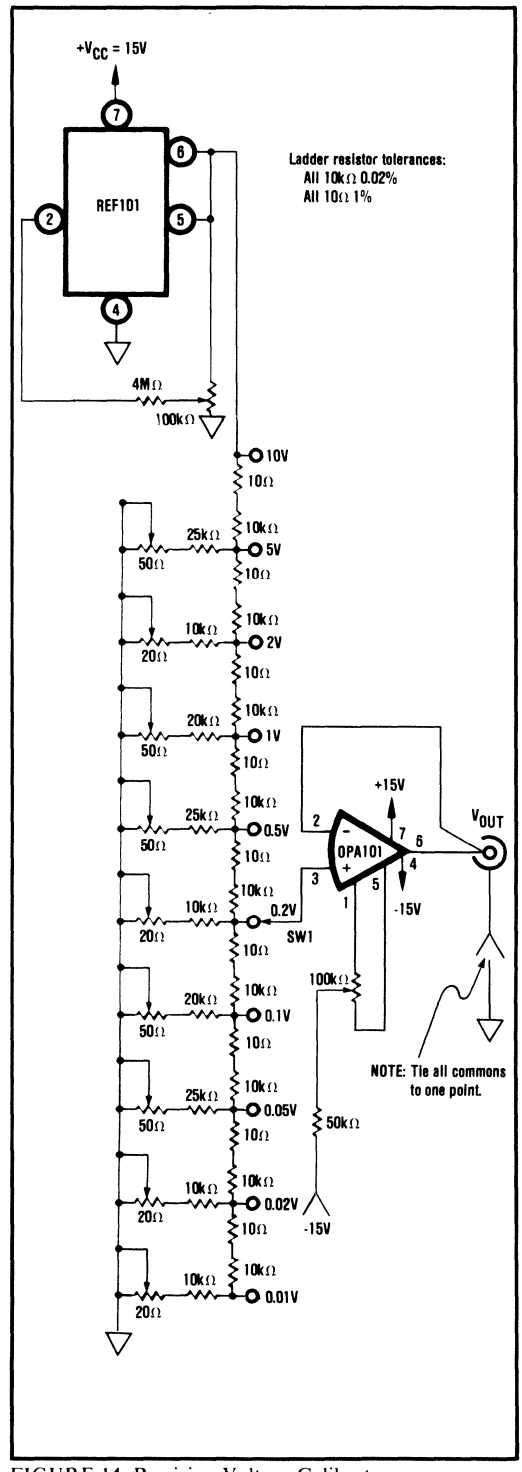


FIGURE 14. Precision Voltage Calibrator.

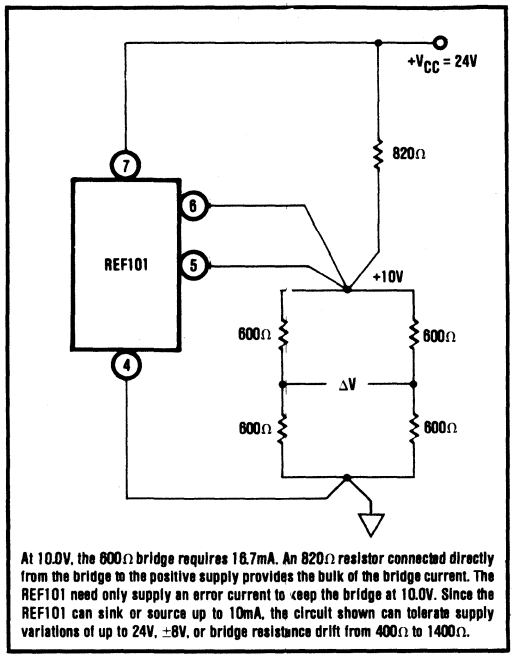


FIGURE 15. +10V Reference with Output Current Boost Using a Resistor to Drive a 600Ω Bridge.

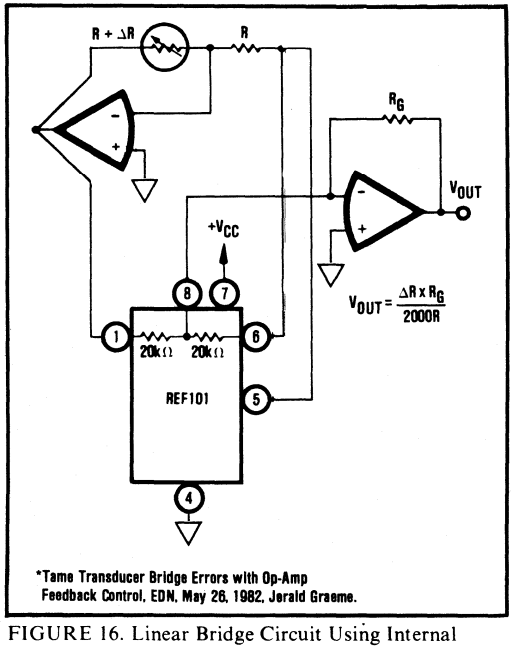


FIGURE 16. Linear Bridge Circuit Using Internal Precision Resistors of the REF101 as the Bridge Completion Network.

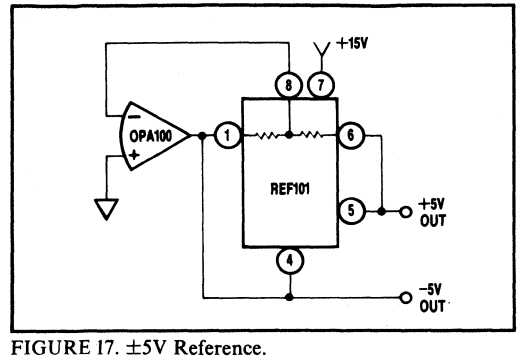


FIGURE 17. ±5V Reference.

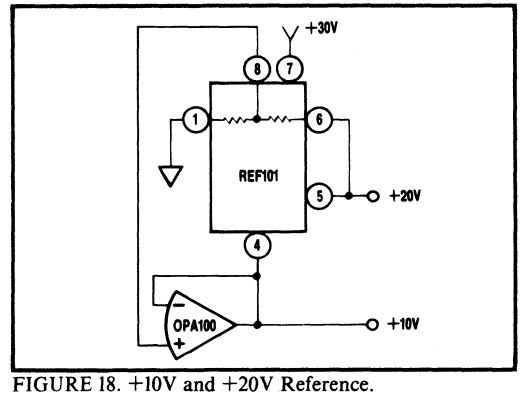


FIGURE 18. +10V and +20V Reference.

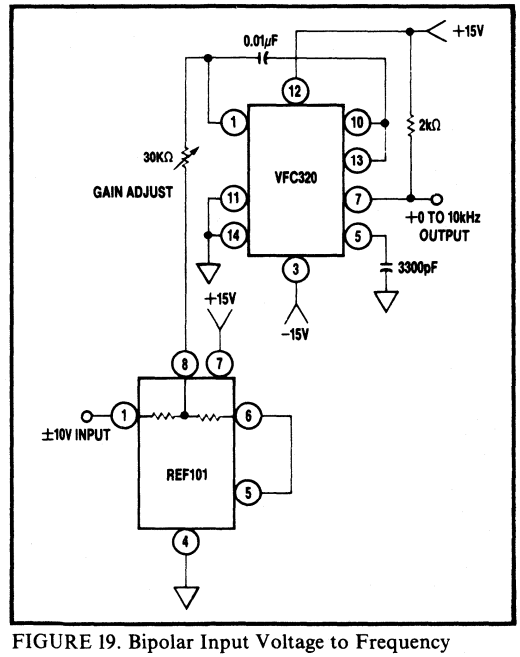
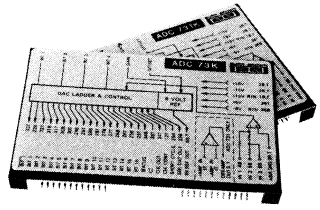


FIGURE 19. Bipolar Input Voltage to Frequency Converter.

BURR-BROWN®



ADC73
ADC731

True 16-Bit
ANALOG-TO-DIGITAL CONVERTER

FEATURES

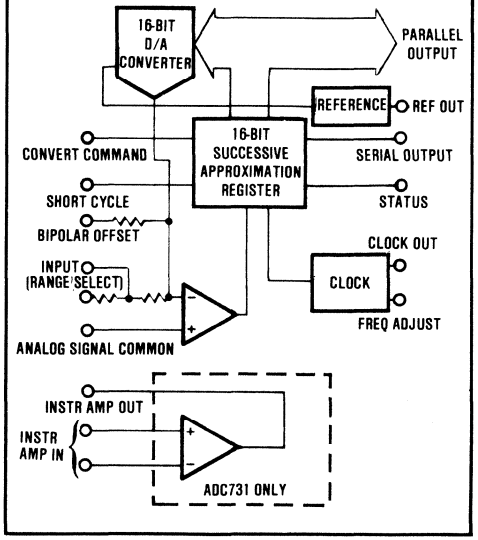
- 16-BIT RESOLUTION WITH TRUE 16-BIT ACCURACY
- LINEARITY ERROR OF LESS THAN ±0.00075% max (K model)
- OPTIONAL UNITY-GAIN INSTRUMENTATION AMPLIFIER INPUT (ADC731)
- FAST CONVERSION TIME - 170μsec max to ±0.00075% accuracy (K models)
- USER-SELECTED INPUT RANGES
- VERY-HIGH PERFORMANCE/PRICE RATIO

DESCRIPTION

The ADC73 and ADC731 are high quality, 16-bit successive approximation analog-to-digital converters that are linear to within ±0.0015% of full scale range (J models) or ±0.00075% of full scale range (K models). They combine state-of-the-art monolithic, hybrid, and discrete technologies to establish a new standard in value for true 16-bit A D converters. Complete with precision internal reference and comparator, ultra-stable clock, and unity-gain instrumentation amplifier input (ADC731), the ADC73 and ADC731 are ready to use. The user-selectable input ranges of ±5V, ±10V, 0 to +10V, and 0 to +20V, short-cycle capability for faster throughput rates, optional instrumentation amplifier input, binary or two's complement codes, parallel and serial outputs, and low price make this versatile converter suitable for a wide range of demanding applications.

Control signals and output data lines are TTL-compatible over the entire operating temperature range. Output data is available as a parallel word or a serial bit stream (MSB first) with corresponding clock and status outputs.

FUNCTIONAL DIAGRAM



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

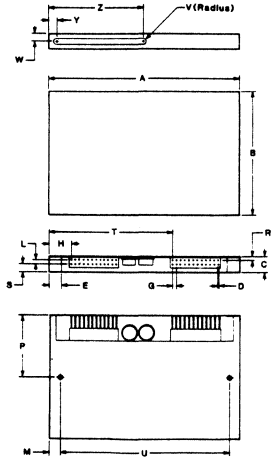
MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			16			16	Bits
INPUT CHARACTERISTICS							
ANALOG							
Voltage Ranges							
Bipolar		±5, ±10			*		V
Unipolar(1)		0 to +10, 0 to +20			*		V
Input Impedance, Direct Input							
0 to +10, ±5V		5			*		kΩ
0 to +20V, ±10V		10			*		kΩ
Differential Amplifier (ADC731 only)							
Input Impedance, Differential		10^{10} || 3			*		Ω || pF
Common-mode		5 x 10^9 || 3			*		Ω || pF
Common-mode Voltage(2)		±(|Vcc| - 3)			*		V
CMRR, ±10V input (3)		76			*		dB
DIGITAL (Convert Command)							
Pulse Width	200			*			nsec
Logic "1" Voltage	2.0			*			V
Current			20			*	μA
Logic "0" Voltage			0.8			*	V
Current			0.4			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(4)		±0.001			*		%
Offset Error(4), Unipolar		±0.001			*		% of FSR
Bipolar		±0.001			*		% of FSR
Linearity Error(5)			±0.0015			±0.00075	% of FSR
Differential Linearity Error(5)		±0.0015	±0.003		±0.00075	±0.0015	% of FSR
Quantization Error			±0.00075			±0.00075	% of FSR
No Missing Codes Temperature Range	+15		+35	*		*	°C
Differential Ground Potential Error(6)							
Gain		0.01			*		LSB/mV
Offset		0.02			*		LSB/mV
Linearity		0.01			*		LSB/mV
Differential Linearity		0.02			*		LSB/mV
3σ Noise, Full Scale (7)		150	300		*	*	μV, p-p
POWER SUPPLY SENSITIVITY							
Offset, +15VDC			±0.0005			*	% of FSR/%ΔV
-15VDC			±0.0001			*	% of FSR/%ΔV
+5VDC			±0.0007			*	% of FSR/%ΔV
Gain, +15VDC			±0.00035			*	% of FSR/%ΔV
-15VDC			±0.0012			*	% of FSR/%ΔV
+5VDC			±0.0004			*	% of FSR/%ΔV
CONVERSION TIME(8)		150	170		*	*	μsec
WARM-UP TIME (To rated accuracy)		15			*		minutes
TEMPERATURE DRIFT (Including Internal Reference)							
Gain			±10			*	ppm/°C
Offset, Unipolar			±2			*	ppm of FSR/°C
Bipolar			±5			*	ppm of FSR/°C
Linearity		±0.5	±2		*	*	ppm of FSR/°C
Differential Linearity		±0.5	±2		*	*	ppm of FSR/°C
LONG TERM STABILITY							
Gain, Exclusive of Reference		±30			*		ppm/10^3 hr
Offset, Exclusive of Reference, Bipolar		±30			*		ppm of FSR/10^3 hr
Unipolar		±5			*		ppm of FSR/10^3 hr
Linearity		±3.7	±7.5		*	*	ppm of FSR/10^3 hr
Reference		±50			*		ppm/10^3 hr

ELECTRICAL (CONT)

MODEL	ADC73J, ADC731J			ADC73K, ADC731K			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS							
DIGITAL							
Data Codes (Positive True Logic)							
Parallel(9)		USB, BOB, BTC			*		
Serial (NRZ)(9)		USB, BOB			*		
Status		Logic "1" During Conversion			*		
Internal Clock							
Frequency		113			*		kHz
Clock Adjust Range		±20			*		%
Logic Levels							
Logic "1" Voltage	2.4			*			V
Current			0.4			*	mA
Logic "0" Voltage			0.4			*	V
Current			3.2			*	mA
INTERNAL REFERENCE							
Voltage	+5.9988	+6.0000	+6.0012	*	*	*	V
Source Current Available for External Loads	4.0			*			mA
Temperature Drift			±5			*	ppm/°C
POWER SUPPLY REQUIREMENTS							
Voltage, +15VDC	+14.5	+15	+15.5	*	*	*	V
-15VDC	-14.5	-15	-15.5	*	*	*	V
+5VDC	+4.75	+5	+5.25	*	*	*	V
Current, +15VDC		---	60		*	*	mA
-15VDC		---	65		*	*	mA
+5VDC		---	130		*	*	mA
POWER DISSIPATION		---	2.5		*	*	W
TEMPERATURE RANGE							
Specification	0		+70	*		*	°C
Storage	-55		+100	*		*	°C

NOTES:
1. Maximum input voltage of ADC731 differential buffer input is ±10V.
2. V_{CC} is value of supply voltage connected to +15V and -15V power supply pins.
3. See CMRR versus frequency performance curve.
4. Adjustable to zero with internal potentiometers. FSR = Full Scale Range.
5. As adjusted at the factory. Periodic recalibration is performed by following the adjustment procedure in the Installation and Operating Instructions.
6. Effect on output of DC voltage differential being present between analog and digital grounds. Measured with 10V Full Scale Range input and up to 175mVDC between grounds.
7. For 20V FSR input voltage. Noise is directly proportional to user-selected FSR.
8. Conversion time can be reduced to 120μsec. See Typical Performance Curves for accuracy versus conversion time. Conversion time and resolution may also be reduced by "short-cycling". See Installation and Operating Instructions.
9. BOB = Bipolar Offset Binary, USB = Unipolar Straight Binary, BTC = Bipolar Two's Complement.

MECHANICAL



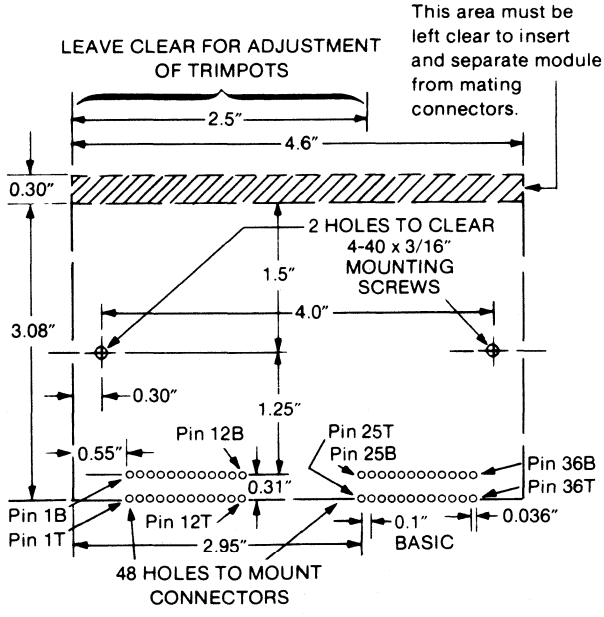
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.590	4.810	116.59	117.09
B	2.990	3.010	75.95	76.45
C	.380	.400	9.65	10.16
D	.022	.028	0.56	0.71
E	.290	.310	7.37	7.87
G	.100 BASIC		2.54 BASIC	
H	.540	.560	13.72	14.22
L	.100 BASIC		2.54 BASIC	
M	.290	.310	7.37	7.87
P	1.46	1.54	37.08	39.11
R	.180	.200	4.57	5.08
S	.090	.110	2.29	2.79
T	2.95	2.97	74.93	75.44
U	3.990	4.010	101.35	101.85
V	.065	.085	1.65	2.16
W	.140	.160	3.56	4.06
Y	.235	.255	5.97	6.48
Z	2.285	2.305	58.04	58.55

PIN DESIGNATIONS

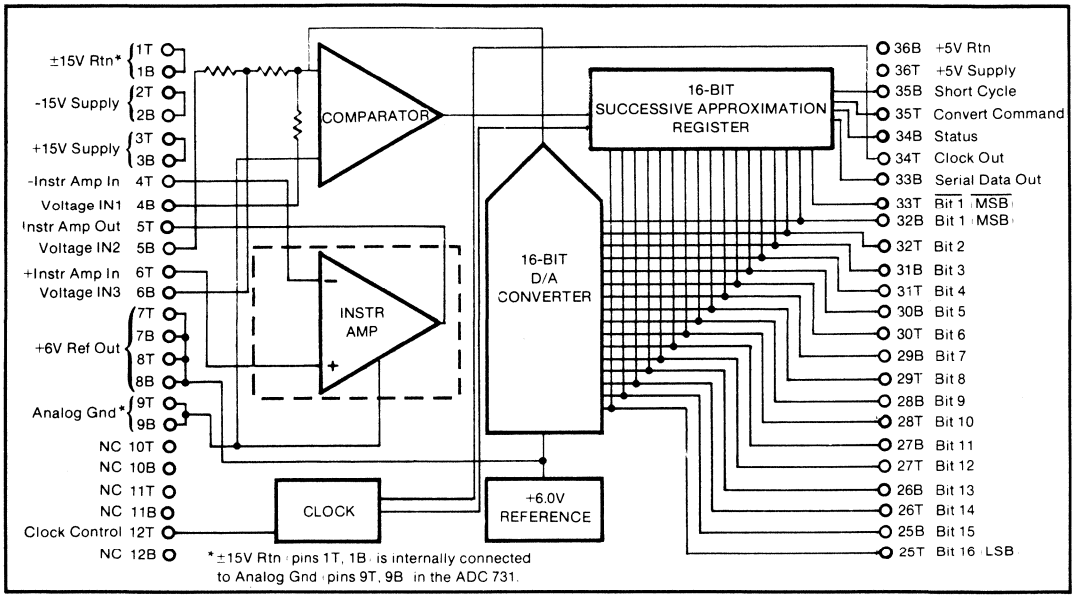
±15V Return(1)	1B	1T	±15V Return(1)	Bit 15	25B	25T	Bit 16 (LSB)
-15V Supply	2B	2T	-15V Supply	Bit 13	26B	26T	Bit 14
+15V Supply	3B	3T	+15V Supply	Bit 11	27B	27T	Bit 12
IN1	4B	4T	-Instr Amp Input	Bit 9	28B	28T	Bit 10
IN2	5B	5T	Instr Amp Output (ADC731 only(3))	Bit 7	29B	29T	Bit 8
IN3	6B	6T	+Instr Amp Input	Bit 5	30B	30T	Bit 6
NC(2)	7B	7T	NC(2)	Bit 3	31B	31T	Bit 4
+6V Ref Out	8B	8T	+6V Ref Out	Bit 1 (MSB)	32B	32T	Bit 2
Analog Gnd(1)	9B	9T	Analog Gnd(1)	Serial Out	33B	33T	Bit 1 (MSB)
NC	10B	10T	NC	Status Out	34B	34T	Clock Out
NC	11B	11T	NC	Short Cycle	35B	35T	Convert Command
NC	12B	12T	Clock Control	+5V Return	36B	36T	+5V Supply

NOTES:
1. ±15V Return (Pins 1T, 1B) is internally connected to Analog Gnd (Pins 9T, 9B) in ADC731.
2. Internally connected to Pins 8T, 8B.
3. Not internally connected on ADC73 models.

PC BOARD MOUNTING DETAILS (component side)

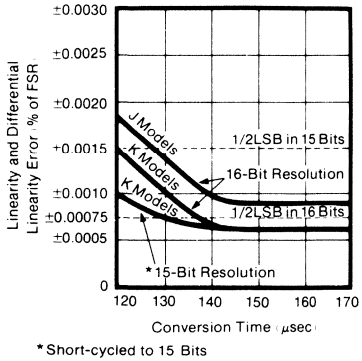


CONNECTION DIAGRAM



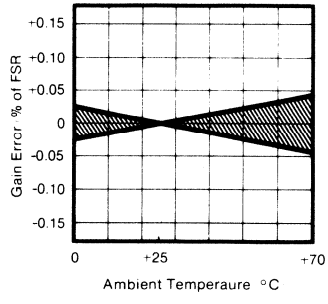
TYPICAL PERFORMANCE CURVES

LINEARITY AND DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME

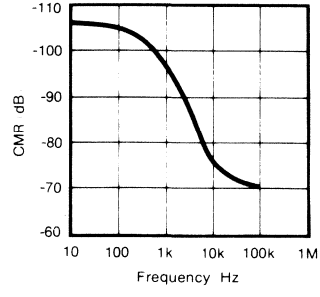


*Short-cycled to 15 Bits

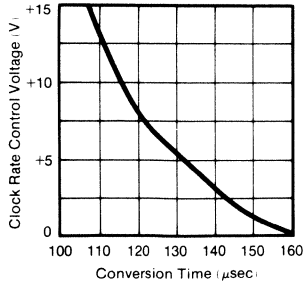
GAIN DRIFT VS AMBIENT TEMPERATURE



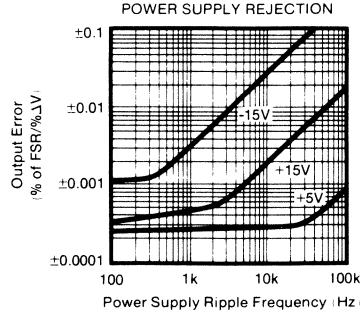
COMMON-MODE REJECTION OF DIFFERENTIAL INPUT BUFFER VS FREQUENCY



CLOCK RATE CONTROL VOLTAGE VS CONVERSION TIME



POWER SUPPLY REJECTION



DISCUSSION OF SPECIFICATIONS AND PERFORMANCE

ACCURACY

The accuracy of a successive approximation A D converter is described by the transfer function shown in Figure 1. All successive approximation A D converters have an inherent quantization error of ±1 2LSB. The remaining errors in the A D converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and the scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Initial gain and offset errors are adjusted to zero at the factory prior to shipment. Periodic recalibration may be performed by the user as needed. Gain drift over temperature rotates the transfer characteristic (Figure 1) about the zero or -FS point (all bits OFF) and offset drift shifts the transfer characteristic left or right. The linearity error has also been adjusted to within ±1 2LSB at the factory and, like gain and offset error, is user adjustable. Linearity error is the deviation of an actual bit transition from ideal transition value at any level over the range of the A D converter. A differential linearity error of ±1 2LSB means that the width of each bit step over the input range of the A/D converter is 1LSB±1/2LSB. The ADC73 and ADC731 are also guaranteed to have no missing codes from +15°C to +35°C.

TIMING CONSIDERATIONS

The timing diagram shown in Figure 2 illustrates by a specific example the timing of the A D logic. It shows how an analog input voltage is converted to the output digital word 0110 0111 0110 1001.

DEFINITION OF DIGITAL CODES

The user may select one of three available codes for the ADC73 or ADC731 parallel output. They are unipolar straight binary (USB) for unipolar input ranges, bipolar offset binary (BOB), and bipolar two's complement (BTC) for bipolar input voltage ranges. Table I shows the LSB voltage, transition voltages and code definitions for each possible analog input signal range for 14-, 15-, and 16-bit resolutions.

Two serial data output codes are available, USB and BOB. The serial data is available as each bit is being converted with the MSB being output first. The serial data is synchronized with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition voltages shown in Table I also apply to the serial data output except for the BTC code.

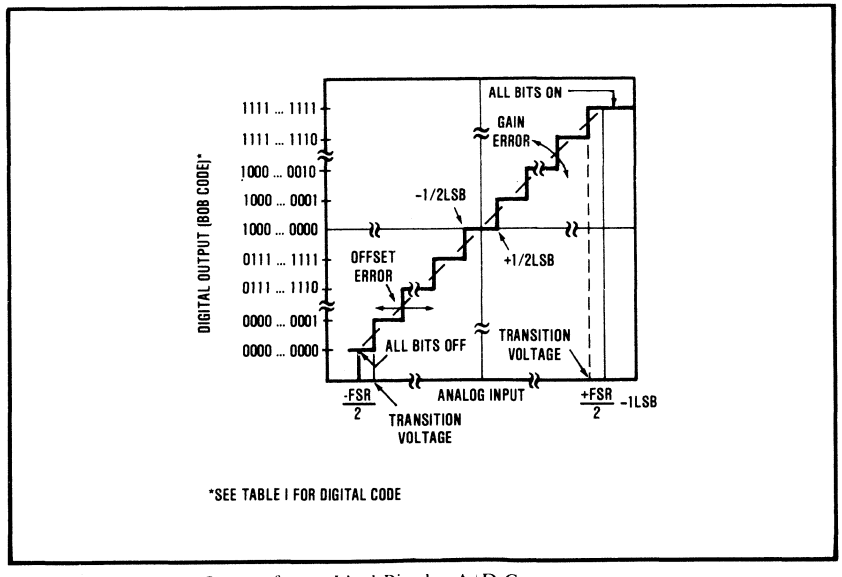
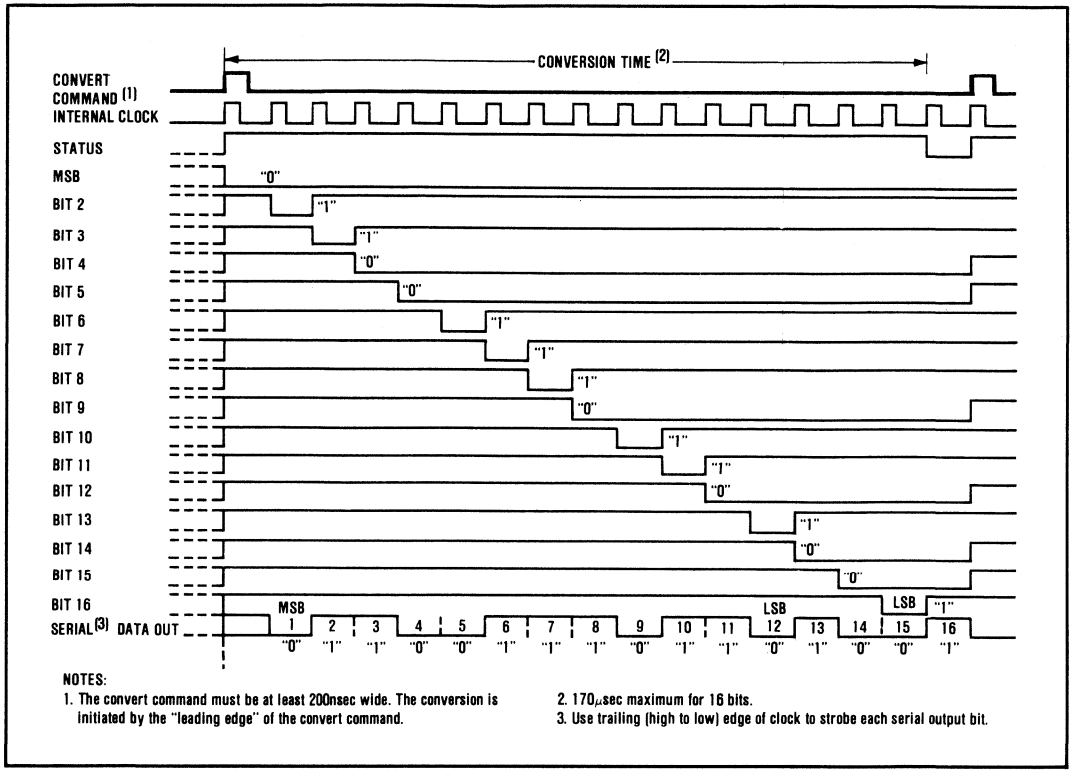


FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.



NOTES:
1. The convert command must be at least 200nsec wide. The conversion is initiated by the "leading edge" of the convert command.
2. 170μsec maximum for 16 bits.
3. Use trailing (high to low) edge of clock to strobe each serial output bit.

FIGURE 2. ADC73 731 Timing Diagram.

TABLE I. Input Voltages, Transition Values, LSB Value and Code Definitions.

INPUT VOLTAGE - RANGE AND LSB VALUES					
Analog Input Voltage Range		±10V	±5V	0 to +10V	0 to +20V
Code Designation		BOB(1) or BTC(2)	BOB(1) or BTC(2)	USB(3)	USB(3)
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 14	1.22mV	610μV	610μV	1.22mV
	n = 15	610μV	305μV	305μV	610μV
	n = 16	305μV	153μV	153μV	305μV
Transition Values(4) MSB LSB					
1111 ... 1111	+Full Scale	+10V-3/2LSB	+5V-3/2LSB	+10V-3/2LSB	+20-3/2LSB
1000 ... 0000	Mid Scale	0±1/2LSB	0±1/2LSB	+5V±1/2LSB	+10±1/2LSB
0000 ... 0000	-Full Scale	-10V+1/2LSB	-5V+1/2LSB	0+1/2LSB	0+1/2LSB

1. BOB = Bipolar Offset Binary
2. BTC = Binary Two's Complement
3. USB = Unipolar Straight Binary
4. Nominal voltages for transition to code specified.

INSTALLATION AND OPERATING INSTRUCTIONS

MOUNTING

Mounting on a printed circuit board is accomplished using the female printed circuit connectors supplied with each A D converter. Mount the A D converter with two #4 external tooth lockwashers and two #4-40 machine screws. Refer to the mounting instructions. Be sure to leave clearance for screwdriver adjustment of the trim potentiometers.

PC LAYOUT CONSIDERATIONS

The metal case (ADC73 and ADC731) is connected internally to the ±15V Rtn pins (1B and 1T). Care must be taken to prevent other printed circuit conductors from making electrical contact with the case. In order to avoid ground loop paths, the case itself should not be connected to any other local power supply returns.

Coupling between digital signal paths and the analog inputs, IN1, IN2, IN3 and +Amp In and -Amp In (ADC731) should be minimized by careful layout separation and or ground plane shielding.

In addition to the power supply connections, other connections to the A D converter should be limited to digital inputs and outputs with a single digital common return path and the analog input.

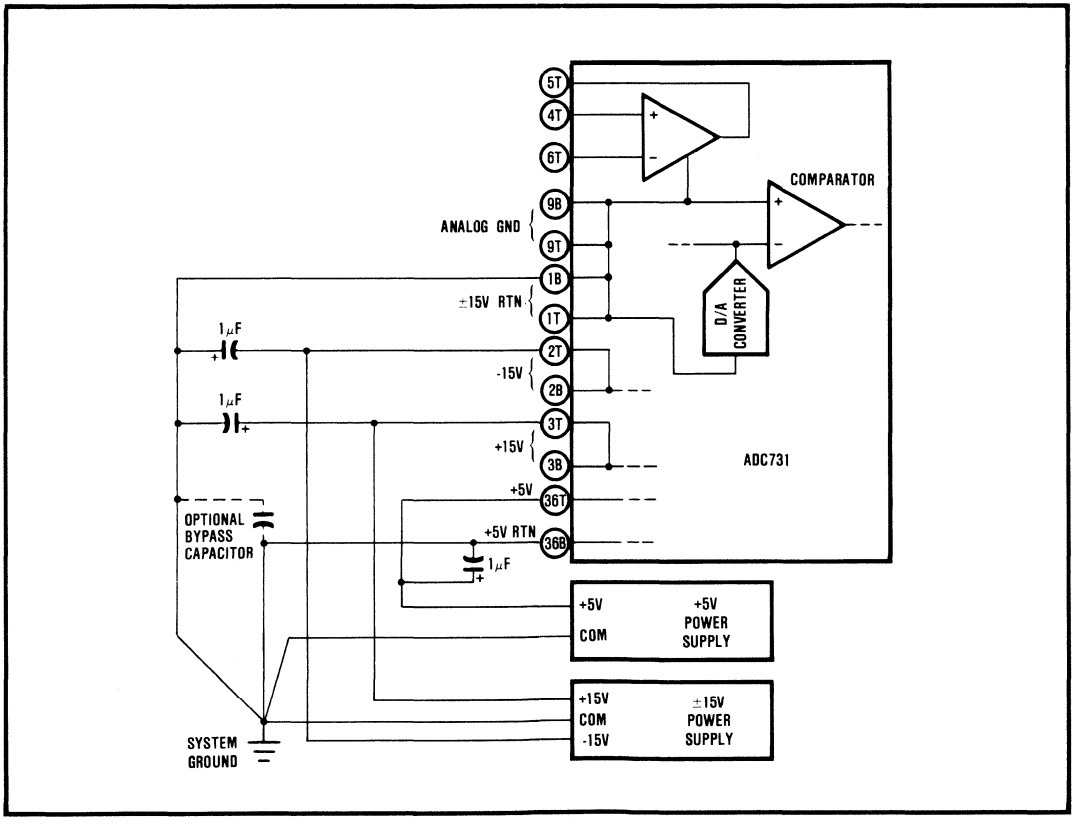


FIGURE 3. ADC731 Power Supply Connections.

POWER SUPPLY CONNECTIONS

ADC731

Analog Gnd (pins 9B, 9T) and ±15V Rtn (pins 1B, 1T) are connected together internally. ±15V Rtn and +5V Rtn (pin 36B) are not connected internally. These supply return lines should be connected together as close to the unit as possible. If ±15V Rtn and +5V Rtn are connected together at a system common point a significant distance from the pins, use a 0.01μF to 0.1μF nonpolarized bypass capacitor between these pins as close to the pins as possible. Refer to Differential Ground Potential Error in Electrical Specification table.

Power supply decoupling capacitors should be used as shown in Figure 3 and located as close as possible to the pins. Use 1μF tantalum or electrolytic capacitors. Parallel electrolytic capacitors with 0.01μF ceramic capacitors for best high frequency decoupling.

ADC73

Analog Gnd and ±15V Rtn pins are not connected internally on this model to permit a separate analog input signal return sense connection. Input signal connections are described in a following section.

Comments made for ADC731 power supply connections also apply to the ADC73. Refer to Figure 4.

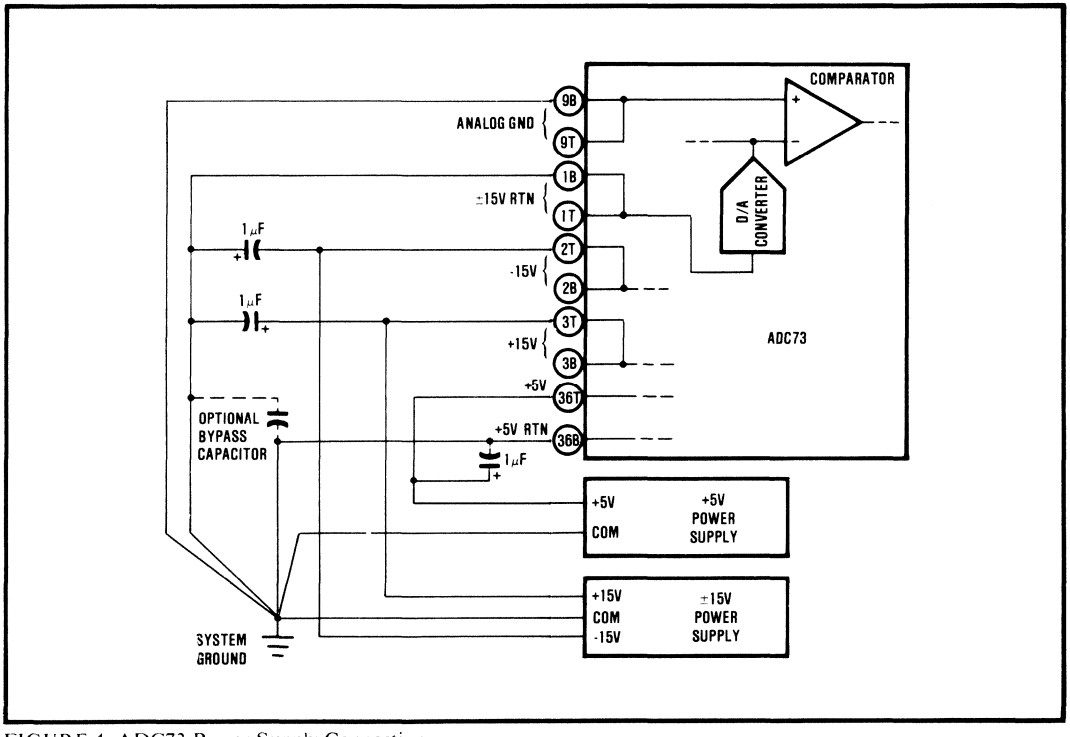


FIGURE 4. ADC73 Power Supply Connections.

SEPARATE POWER SUPPLIES

Because the effectiveness of high resolution A/D converters can be reduced by small amounts of noise, separate floating supplies may be needed for applications in environments with high electrical noise. These supplies and their return paths should be connected to the A/D converter only. Some experimentation with extra shielding and alternative return configurations may be necessary in extreme circumstances.

INPUT CONNECTIONS

ADC73

Analog input signals to ADC73 are connected directly to low impedance inputs (5kΩ and 10kΩ). The user may select unipolar or bipolar, 10V or 20V full scale ranges as illustrated in Figure 5.

ADC731

ADC731 has a precision high impedance differential input buffer. The user may select a unipolar range of 0 to +10V or bipolar ranges of ±5V or ±10V as illustrated in Figure 6. Note that signal input voltage V_{IN} plus the common-mode voltage is limited to ±10V for the bipolar connection and +10V for the unipolar connections.

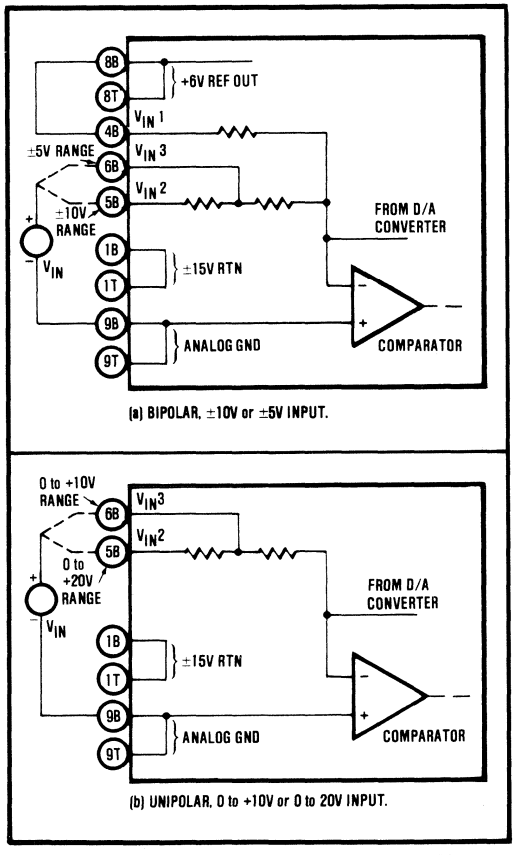


FIGURE 5. Signal Input Connections for ADC73.

CALIBRATION

The relative accuracy of ADC73 and ADC731 is adjusted to within specification at the factory. Offset and Gain may need to be adjusted after the A/D converter is installed and, after extended periods of time, recalibration will be necessary.

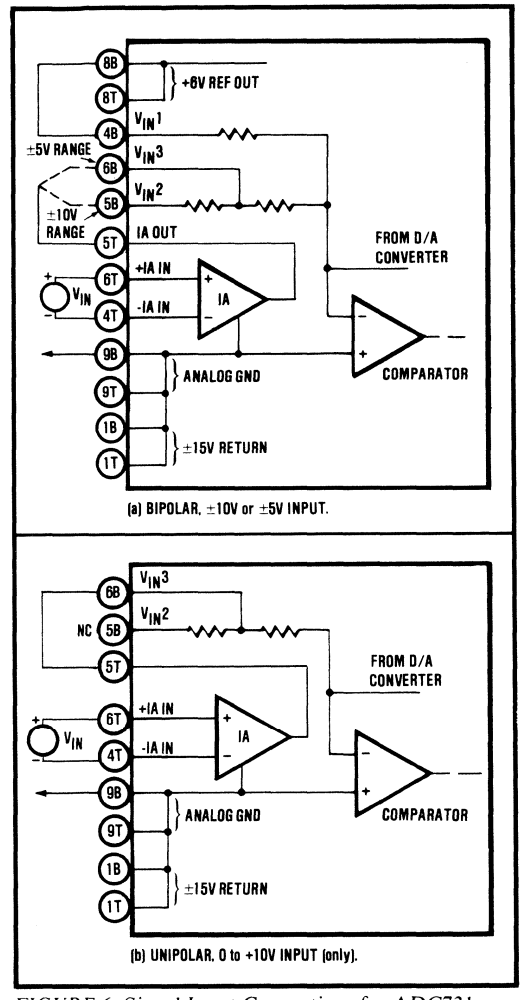


FIGURE 6. Signal Input Connections for ADC731.

Six potentiometers are built into the ADC73 and ADC731 for adjusting Offset (1 potentiometer), Gain (1 potentiometer), and Linearity (4 potentiometers). Linearity is adjusted in the first 4MSB's by adjusting the currents in bits 1(MSB), 2, 3, and 4. Refer to Table II for the transition voltages to be applied to the input appropriate to the input range being used. All input voltages should be set within ±10μV of the ideal voltage.

Procedure for full calibration (Offset, Linearity, and Gain):

1. Set the input voltage to the transition voltage for offset calibration. Adjust the Offset potentiometer until the transition to 0001_{16} from 0000_{16} occurs 50% of the time with repeated conversions.
2. Set the input to the transition voltage for the Gain Cal adjustment listed in Table II. Adjust the Gain potentiometer until the transition to $0FFF_{16}$ from $0FFE_{16}$ occurs 50% of the time with repeated conversions. If bit 4 should turn on such that the codes $1FFF_{16}$ and $1FFE_{16}$ occur, adjust potentiometer labeled bit 4 so that bit 4 (pin 31T) does not turn on.
3. Set the input to the bit 4 transition voltage of Table II. Adjust the potentiometer labeled bit 4 until the transition to 1001_{16} from 1000_{16} occurs 50% of the time with repeated conversions.
4. Set the input to the transition voltage for bit 3. Adjust potentiometer labeled bit 3 until the transition to 2001_{16} from 2000_{16} occurs 50% of the time with repeated conversions.
5. Set the input to the transition voltage for bit 2. Adjust the potentiometer labeled bit 2 until the transition to 4001_{16} from 4000_{16} occurs 50% of the time with repeated conversions.
6. Set the input to the transition voltage for bit 1. Adjust the potentiometer labeled bit 1 until the transition to 8001_{16} from 8000_{16} occurs 50% of the time with repeated conversions.
7. Set the input to the transition voltage for Gain calibration. Adjust the potentiometer labeled Gain until transition to $FFFF_{16}$ from $FFFE_{16}$ occurs 50% of the time with repeated conversions.

If adjusting only Offset and Gain, perform only steps 1 and 7, in that order.

TABLE II. Calibration Values for ADC73 and ADC731.

Input Voltage Range	0 to +10V	0 to +20V	±5V	±10V
POTENTIOMETER ADJUST Transition Codes(1)	**Transition voltages for 16-bit resolution**(2)			
Offset to 0001_{16} from 0000_{16}	0.000076V	0.000153V	-4.99924V	-9.999847V
Gain Cal(3) to $OFFF_{16}$ from $OFFE_{16}$	0.624771V	1.249542V	-4.375229V	-8.750458V
Bit 4 to 1001_{16} from 1000_{16}	0.625076V	1.250153V	-4.374924V	-8.7498747V
Bit 3 to 2001_{16} from 2000_{16}	1.250076V	2.500153V	-3.749924V	-7.499847V
Bit 2 to 4001_{16} from 4000_{16}	2.500076V	5.000153V	-2.499924V	-4.999847V
Bit 1 to 8001_{16} from 8000_{16}	5.000076V	10.000153V	0.000076V	0.000153V
Gain to $FFFF_{16}$ from $FFFE_{16}$	9.999771V	19.999542V	4.999771V	9.999542V

1. Positive true codes, Bipolar Offset Binary or Unipolar Straight Binary.
2. Voltages given are the nominal value for transition to the code shown.
3. This transition code used only prior to linearity error adjustment.

OPTIONAL CONVERSION TIME ADJUSTMENT

ADC73 and ADC731 may be operated at faster or slower conversion rates by connecting the Clock Control pin (12T) to a positive voltage between 0 and +15V as shown in Figure 7. The conversion time range is typically from 120μsec (12T at +15V) to 190μsec (12T tied to +15V Rtn), see Typical Performance Curves. If pin 12T is left open, the conversion time is typically 150μsec. Figure 7 illustrates the circuit used for conversion rate control. The potentiometer is a non-critical component.

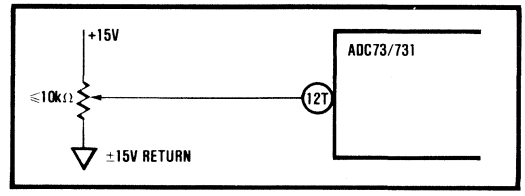


FIGURE 7. Clock Rate Control.

CHANGING RESOLUTION BY SHORT CYCLING

The ADC73 and ADC731 may be short cycled to lower resolutions and higher conversion rates by connecting the Short Cycle pin (35B) to the appropriate bit output as listed in Table III.

TABLE III. Connections for Short-Cycling Resolution Conversions.

Resolution (bits)	16	15	14	13	12
Connect pin 35B* to	Open	25T	25B	26T	26B
Connect pin 12T to	Open	Open	Open	Open	Open
Typical Conversion Time with pin 12T open μsec	150	141	132	123	114

*For resolutions less than 16 bits also connect pin 35B through a 2kΩ resistor to +5V.

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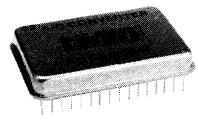


ADC803

High-Speed ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 12-BIT RESOLUTION
- ±0.015% LINEARITY AND DIFFERENTIAL LINEARITY ERROR MAXIMUM (C GRADE)
- NO MISSING CODES −25°C TO +85°C
- 32-PIN METAL PACKAGE
- CONVERSION TIME: 500nsec, 8 bits
  670nsec, 10 bits
  1.5μsec, 12 bits

DESCRIPTION

The ADC803 is a high speed successive approximation analog-to-digital converter utilizing state-of-the-art IC and laser-trimmed thin film components.

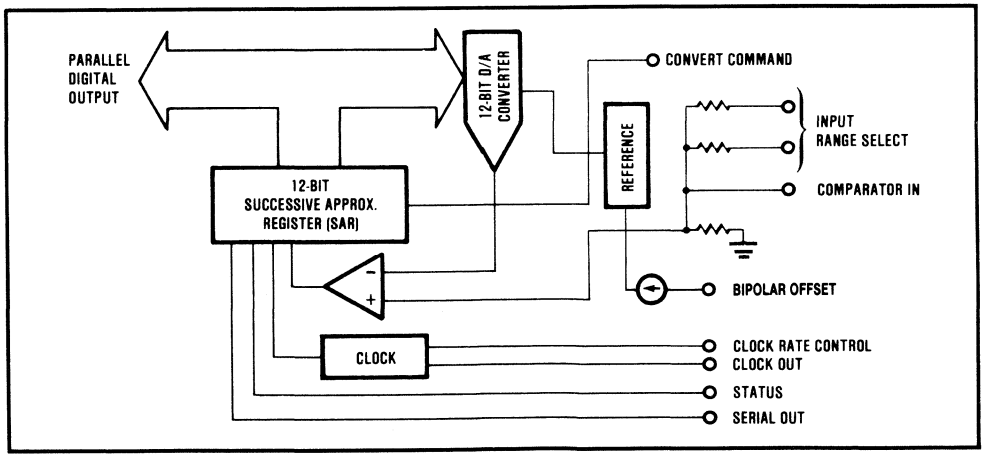
It is complete with internal reference, clock, and comparator and is packaged in a 32-pin metal package. Conversion time is set at the factory to 1.5μsec.

With user-adjusted conversion time set at 1μsec, ±1LSB accuracy can be achieved. The gain and offset errors may be externally-trimmed to zero.

Internal scaling resistors are provided for the selection of analog signal input ranges of 0V to -10V, ±5V, and ±10V.

Output data is available in a serial or parallel format. Output codes available are complementary binary for unipolar inputs and bipolar offset binary for bipolar inputs.

All digital inputs and outputs are TTL-compatible. Power supply requirements are ±15V and +5V.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, rated power supplies, 1.5μsec conversion time, and after 6-minute warm-up unless otherwise noted.

MODEL	ADC803CM			ADC803BM			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			12	Bits
INPUTS							
ANALOG							
Voltage Ranges							
Bipolar		±5, ±10			"		V
Unipolar		0 to -10			"		V
Impedance							
-10V to 0V, ±5V		1.4			"		kΩ
±10V		2.4			"		kΩ
DIGITAL							
Convert Command	Negative pulse 50nsec wide (min) trailing edge (0 to 1) initiates conversion						
Logic Loading			4			"	TTL Loads
TRANSFER CHARACTERISTICS							
ACCURACY							
Gain Error(1)		±0.04	±0.1		±0.08	±0.2	%
Offset Error(1)							
Unipolar		±0.05	±0.2		±0.07	±0.3	% of FSR(2)
Bipolar		±0.02	±0.1		"	±0.2	% of FSR
Linearity Error							
1.5μsec Conversion Time		±0.012	±0.015			±0.020	% of FSR
1.0μsec Conversion Time		±0.015	±0.020		±0.020		% of FSR
Differential Linearity Error							
1.5μsec Conversion Time		±0.012	±0.015			±0.020	% of FSR
1.0μsec Conversion Time			±0.024		±0.024		% of FSR
Inherent Quantization Error		1/2			"		LSB
POWER SUPPLY SENSITIVITY							
Gain and Offset							
+15VDC		±0.0036			"		% of FSR/%V_{CC}
-15VDC		±0.0005			"		% of FSR/%V_{CC}
+5VDC		±0.001			"		% of FSR/%V_{DD}
Conversion Time							
+15VDC		±0.7			"		%/%V_{CC}
-15VDC		None			"		%/%V_{CC}
+5VDC		±0.8			"		%/%V_{DD}
CONVERSION TIME							
Factory Set	1.3		1.5			"	μsec
Range of Adjustment(3)	0.8		2.2	"		"	μsec
DRIFT							
Gain		±10	±30		±15	"	ppm of FSR/°C
Offset							
Unipolar		±2	±7		±3	"	ppm of FSR/°C
Bipolar		±3	±10		±5	"	ppm of FSR/°C
Linearity Error, -25°C to +85°C							
1.5μsec Conversion Time		±0.012	±0.018			±0.024	% of FSR
1.0μsec Conversion Time		±0.015			±0.020		% of FSR
Differential Linearity Error, -25°C to +85°C							
1.5μsec Conversion Time		±0.012	±0.018			±0.024	% of FSR
1.0μsec Conversion Time		±0.015			±0.024		% of FSR
Conversion Time		±0.1			"		%/°C
No Missing Code Temp. Range							
1.5μsec Conversion Time	-25		+85	"		"	°C
OUTPUT							
DIGITAL DATA							
Parallel							
Output Codes							
Unipolar			Complementary Straight Binary				
Bipolar			Bipolar Offset Binary				
Output Drive	6				"		TTL Loads
Serial Data Codes (NRZ)			Same as Parallel (MSB first)				
Output Drive	6				"		TTL Loads
Status			Logic "1" during Conversion				
Status Output Drive	6				"		TTL Loads
Internal Clock							
Clock Output Drive	3				"		TTL Loads
Frequency (without external clock adjustment)		8			"		MHz

ELECTRICAL (CONT)

MODEL	ADC803CM			ADC803BM			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY REQUIREMENTS							
Power Consumption							
Rated voltage, Analog ($\pm V_{CC}$)	±14.25	±15.0	±15.75	*	*	*	VDC
Digital (V_{DD})	+4.75	+5.0	+5.25	*	*	*	VDC
Supply Drain, +15V		+27	+32		*	*	mA
-15V		-38	-55		*	*	mA
+5V		+180	+210		*	*	mA
TEMPERATURE RANGE (AMBIENT)							
Specification	-25		+85	*		*	°C
Storage	-55		+125	*		*	°C

*Specification same as for ADC803CM

NOTES:
1. Adjustable to zero. See Optional Gain and Offset Adjustment section.
2. FSR means Full Scale Range. For example, unit connected for ±10V has 20V FSR.
3. See Optional Clock Rate Control section. For faster conversion time at less resolution, see section on External Short Cycle.

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage To Analog Common...±18V

Digital Supply Voltage To Digital Common....+7V

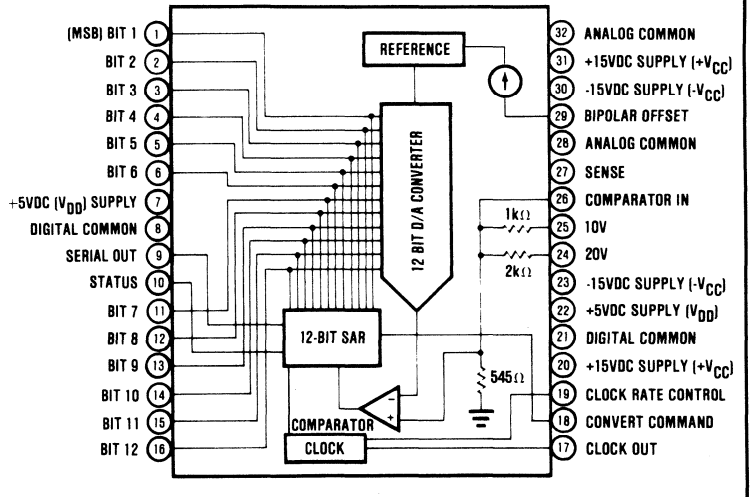
Digital Controls Inputs.....+5.5V

Analog Inputs.....±15V

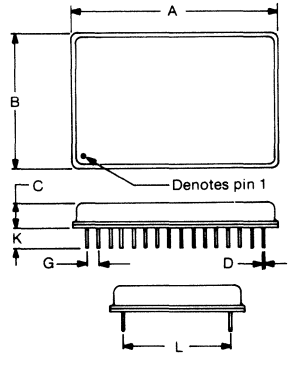
Operating Temperature
- Ambient.....+85°C
- Case.....+125°C

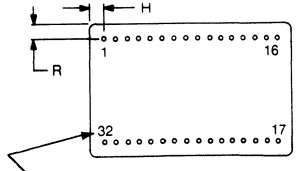
Storage Temperature....+125°C

CONNECTION DIAGRAM



MECHANICAL





Pin numbers shown for reference only. Numbers may not be marked on package.

Pin 1 can be identified from bottom of unit by either a contrasting color of glass seal or a square corner. Case is tied to Digital Common.

NOTE: Leads in true position within 0.10" (0.25mm) R at MMC at seating plane. Pin 8 connected to case.

PINS: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2)
CASE: Kovar, Nickel plated
HERMETICITY: Gross Leak Test
MATING CONNECTOR: 2302MC Set of two 16-pin strips
WEIGHT: 13 grams (0.46 oz.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.720	1.760	43.69	44.70
B	1.120	1.160	28.45	29.46
C	.170	.250	4.32	6.35
D	.016	.021	0.41	0.53
G	.100 BASIC		2.54 BASIC	
H	.100	.140	2.54	3.56
K	.150	.300	3.81	7.62
L	.900 BASIC		22.86 BASIC	
R	.100	.140	2.54	3.56

THEORY OF OPERATION

The accuracy of a successive approximation analog-to-digital converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry matching and tracking properties of the ladder and scaling networks, power supply rejection, reference errors and the dynamic errors of the DAC and comparator. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the transfer function (Figure 1) about the zero point and Offset drift shifts the transfer function left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB, ±1/2LSB. The ADC803 is guaranteed to have no missing codes over the specified temperature range.

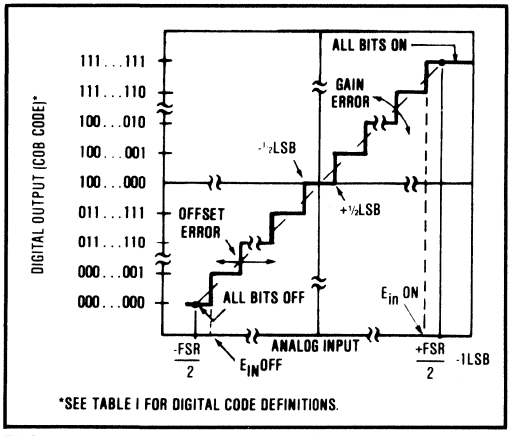


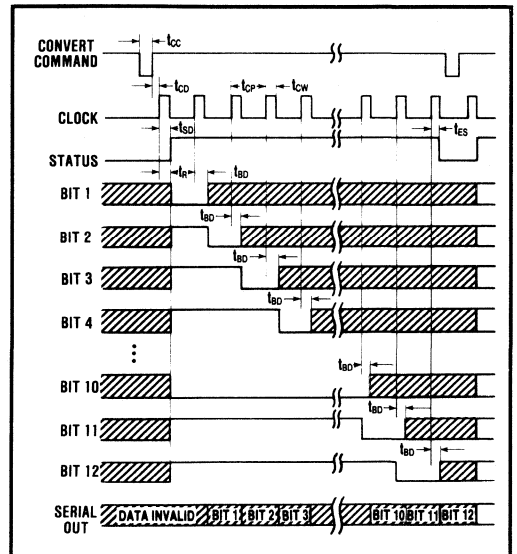
FIGURE 1. Input versus Output for an Ideal Bipolar A/D Converter.

TIMING CONSIDERATIONS

The timing diagram (Figure 2) shows the relationship between the convert command, clock and outputs. The digital output word is positive true logic for bipolar operation and complementary logic for unipolar operation.

The following are some important notes on the ADC803 timing. The times given are typical unless otherwise noted. Nominal maximum and minimum times are also given in Figure 2.

1. When power is first applied, the status of the ADC803 will be undetermined. A CONVERT COMMAND must be applied to initialize the ADC803.



Time Period	Min* (nsec)	Max* (nsec)
t_{CC}	50	—
t_{CD}	15	40
t_{CP}**	100	125
t_{CW}	17	25
t_{SD}	10	38
t_R	10	38
t_{BD}	10	38
t_{ES}	10	38

*Nominal
**Without external adjustment

FIGURE 2. ADC803 Timing Diagram.

2. The CONVERT COMMAND must be low at least 50nsec prior to the "0" to "1" edge that starts a conversion.
3. The clock runs continuously when the initial CONVERT COMMAND goes high and whenever the CONVERT COMMAND is high thereafter. It does not run when CONVERT COMMAND is low. It may be beneficial to keep CONVERT COMMAND low except during conversions to limit the digital noise induced in the ground and power supply lines.
4. The clock starts 25nsec after the "0" to "1" transition of the CONVERT COMMAND.
5. **Parallel Output Data:** The Successive Approximation Register (SAR) is reset 26nsec after the leading edge of the first clock period in the conversion cycle. The MSB is set to logic "0" and all other bits are set to logic "1". The bits are determined in succession starting with the MSB, Bit 1, as shown in Figure 2. Each bit will be valid 26nsec after its corresponding clock pulse.
6. **Serial Output Data:** The serial output is indeterminate until Bit 1 is valid, which occurs 26nsec after

the leading edge of the second clock pulse. The remaining bits (Bits 2 through 12) are valid in succession for one clock period each beginning 26nsec after the leading edge of each clock pulse.

7. STATUS goes high 26nsec after the leading edge of the first clock pulse and goes low 18nsec after the leading edge of the last clock pulse.
8. Bit 12 will become valid at about the same time STATUS goes low and a new conversion can be initiated at anytime after the output data has been read.
9. The converter may be restarted during a conversion. When CONVERT COMMAND makes a "0" to "1" transition after the minimum set-up time, the SAR will be reset and a new conversion will start regardless of the state of the converter prior to the CONVERT COMMAND being received.

Figures 3, 4, and 5 are photographs of the actual pulse shapes and relationships.

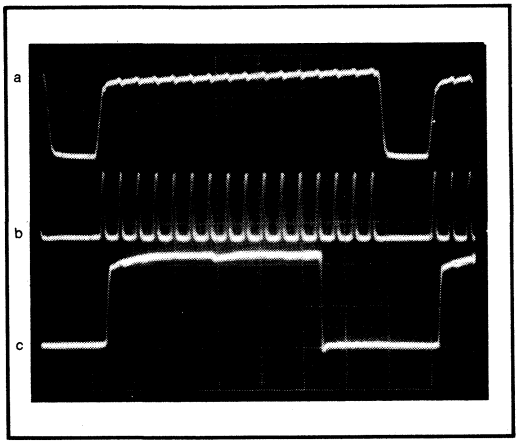


FIGURE 3. Photo of (a) Convert Command, (b) Clock, and (c) Status (200nsec/div).

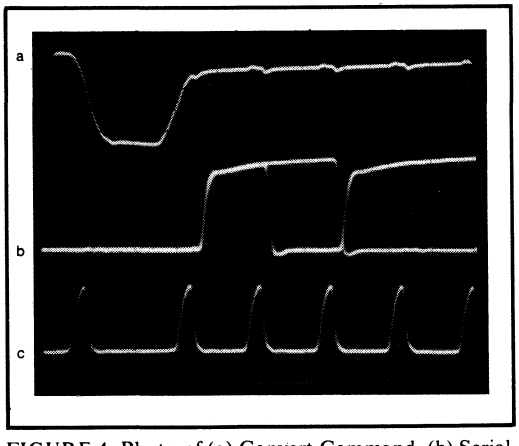


FIGURE 4. Photo of (a) Convert Command, (b) Serial Out, and (c) Clock (50nsec/div).

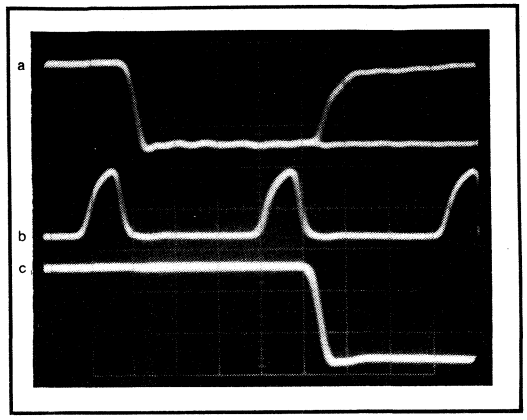


FIGURE 5. Photo of (a) Bit-12 Data (Parallel), (b) Clock, and (c) Status (20nsec/div).

DIGITAL CODES

Parallel Data

Two binary codes are available on the ADC803 parallel output; they are complementary straight binary (Logic "0" true) for unipolar input signal ranges and bipolar offset binary (Logic "1" true) for bipolar input signal ranges. Binary two's complement may be obtained for bipolar input ranges by inverting the MSB. It should be noted that for unipolar input ranges -10 volts is full scale.

Table I shows the LSB, transition values, and code definitions for each possible analog signal range.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Analog Input Voltage Range	±10V	±5V	0 to -10V
Code Designation	BOB[1] or BTC[2]	BOB or BTC	CSB[3]
One Least Significant Bit - LSB	4.88mV	2.44mV	2.44mV
Transition Values MSB LSB[4]			
000...000 ↔ 000...001	-10V + 1/2LSB	-5V + 1/2LSB	-10V + 3/2LSB
011...111 ↔ 100...000	-1/2LSB	-1/2LSB	-5V + 1/2LSB
111...110 ↔ 111...111	+10V - 3/2LSB	+5V - 3/2LSB	-12LSB

NOTES: 1. BOB = Bipolar Offset Binary.
2. BTC = Binary Two's Complement (obtained by inverting the most significant bit (pin 1).
3. CSB = Complementary Straight Binary.
4. Voltages given are the nominal value for the transition from the next lower code.

Serial Data (NRZ)

Two binary codes are available on the serial output line; they are complementary straight binary (CSB) for unipolar input ranges and bipolar offset binary (BOB) for bipolar input signal ranges. The serial data is available

only during conversion and appears with the MSB first. See the timing diagram and discussion under "timing considerations" for more detailed information.

The LSB and transition values shown in Table I. also apply to the serial data output, except serial output does not have a BTC code.

DISCUSSION OF SPECIFICATIONS

The ADC803 is specified to meet critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are Linearity, Drift, Gain and Offset errors, and Conversion speed effects on accuracy. This ADC is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to typically ±0.05% of FSR at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown in Figures 10, 11, and 12.

ACCURACY VERSUS CONVERSION TIME

In successive approximation A/D converters, the conversion time affects Linearity and Differential Linearity errors. Conversion time and its effect on Linearity and Differential Linearity errors for the ADC803 are shown in Figure 6.

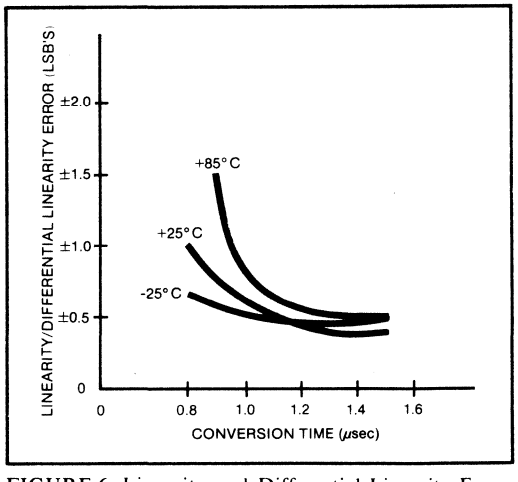


FIGURE 6. Linearity and Differential Linearity Error versus Conversion Time.

POWER SUPPLY SENSITIVITY

Changes in the DC power supply voltages will affect accuracy. Normally, regulated power supplies with 1% or less ripple are recommended for use with this ADC. See Layout Precautions, Power Supply Decoupling, and Figure 7.

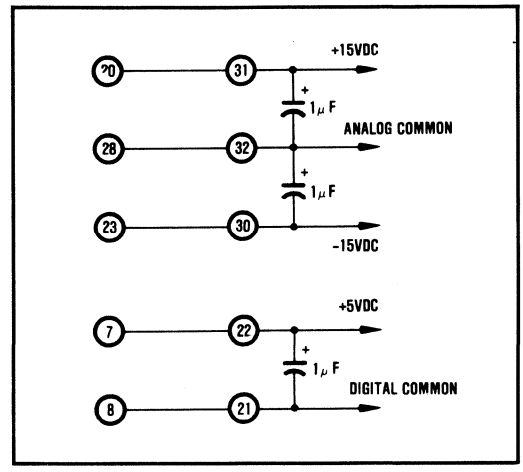


FIGURE 7. Recommended Power Supply Decoupling.

LINEARITY ERROR

Linearity error is not adjustable by the user and is the most meaningful indicator of A/D converter accuracy. Linearity is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity describes the step size between transition values. A Differential Linearity error of ±1/2LSB indicates that the size of any step may not vary from 1LSB by more than ±1/2LSB.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

The ADC803 is a high speed analog-to-digital converter which requires more layout precautions than general purpose products.

The ADC803 has two pins for analog common, two pins for digital common, and two pins for each power supply input. Each pair of these pins must be connected together externally. The connection between the digital supply pins and the connection between the digital common pins must be as short as possible. The analog and digital commons are not connected together internally in the ADC803, but should be connected together externally to a ground plane.

Connecting all commons to a ground plane at the ADC803 is the best method to minimize noise and dissipate heat. Pin 8 (Digital Common) is internally connected to the case.

The ADC803 also has an analog common Sense input (pin 27) for the analog input. This sense pin must be

connected to analog common as close to the input signal source as possible or connected to the ground plane. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog inputs and digital lines should be minimized by careful layout. Special attention should be taken to ensure that the clock noise on the +5V supply line does not couple into the analog inputs.

The Comparator input (pin 26) is extremely sensitive to noise. Any connection to this point should be as short as possible and shielded by analog common or ±15VDC supply patterns. The Clock Output (pin 17) is sensitive to stray capacitance; capacitance on this pin could alter the clock wave shape.

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with 1μF tantalum capacitors as shown in Figure 8 to obtain noise-free operation. These capacitors should be located close to the ADC.

INPUT SCALING

The analog input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signals as shown in Table II. See Figure 8 for circuit details.

TABLE II. ADC803 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 29 To	With Gain Adjust	Connect Pin 24 To	Connect Pin 25 To
±10V	BOB or BTC*	26	Yes	50Ω resistor in series with input signal	Gain Adjust Potentiometer
			No	Input Signal	Analog Common
±5V	BOB or BTC*	26	Yes	Gain Adjust Potentiometer	25Ω resistor in series with input signal
			No	Analog Common	Input Signal
0 to −10V	CSB	Analog Common	Yes	Gain Adjust Potentiometer	25Ω resistor in with input signal
			No	Analog Common	Input Signal

*Obtained by inverting MSB (pin 1) externally.

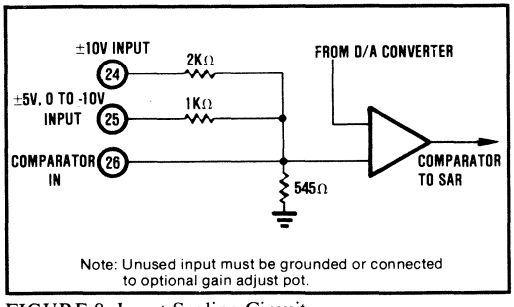


FIGURE 8. Input Scaling Circuit.

OUTPUT DRIVE

All ADC803 outputs except the clock will drive six TTL loads; the clock will drive three TTL loads. If long digital lines must be driven, external logic buffers are required particularly for the clock which is sensitive to capacitive loading.

INPUT IMPEDANCE

The source impedance to the ADC803 should be low, such as the output of an op amp, to avoid any errors due to the relatively low input impedance of the ADC803.

If this impedance is not low, a buffer amplifier should be added between the input signal and the ADC803 input as shown in Figure 9.

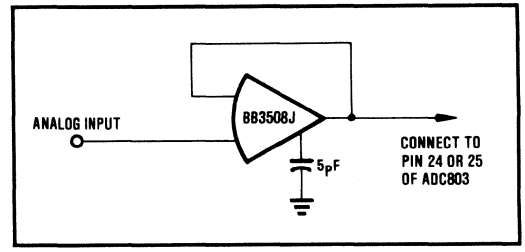


FIGURE 9. Source Impedance Buffering.

A common problem with successive approximation A/D converters is the transients in input current caused by the comparator input being switched back and forth. This requires a fast settling amplifier to drive the input.

The ADC803 comparator is connected in a differential mode (see Figure 8), greatly reducing the size of the input transients. The user, therefore, may use a low cost wideband monolithic amplifier to drive the ADC803. The small signal settling time of the amplifier should be less than 100nsec.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external trim potentiometers connected to the ADC as shown in Figures 10, 11, and 12. For proper gain adjust range a series resistor must be connected to the analog input pin as specified in Table II and shown in Figures 11 and 12. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for minimum drift over temperature and time. All resistors should be ±1% metal film or better. If the Offset adjust is not used, pin 26 should be left open except for bipolar operation when it is connected to pin 29. If the Gain adjust is not used, the unused input (pin 24 or 25) must be grounded to meet specified gain accuracy.

Adjustment Procedure

Refer to Table I for LSB voltages and transition values.

Unipolar offset - connect the offset potentiometer and resistors as shown in Figure 11, sweep the input through

the end point transition voltage, from 111...110 to 111...111. Adjust the Offset potentiometer until the actual end point transition voltage occurs at -1/2LSB.

Bipolar offset - connect the offset potentiometer and resistors as shown in Figure 10. Sweep the input through zero and adjust the offset potentiometer until the transition from 0111 1111 1111 to 1000 0000 0000 occurs at −1/2LSB.

Gain - connect the Gain potentiometer as shown in Figure 11 or 12. Sweep the input through the end point transition voltage that should cause an output transition from 000...000 to 000...001. Adjust the Gain potentiometer until this transition occurs at the correct end point transition voltage as given in Table I.

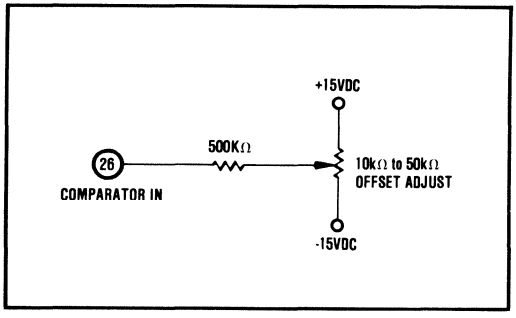


FIGURE 10. Optional Offset Adjust

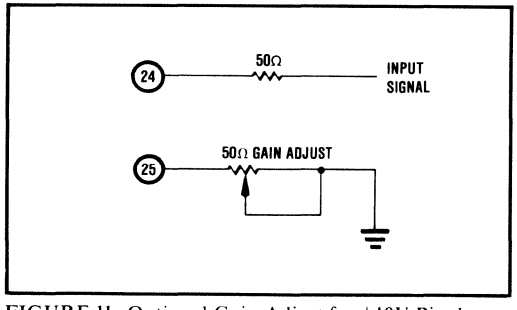


FIGURE 11. Optional Gain Adjust for ±10V Bipolar Operation.

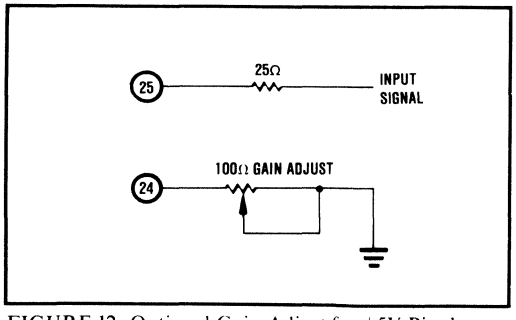


FIGURE 12. Optional Gain Adjust for ±5V Bipolar or 0 to -10V Unipolar Operation.

OPTIONAL CLOCK RATE CONTROL

The clock is factory-set for a conversion time between 1.3μsec and 1.5μsec. By use of the optional Clock Rate Control as shown in Figure 13, the Conversion time can be adjusted down to 0.8μsec for 12-bit resolution. If the optional Clock Rate Control is not used, pin 19 should be left open. Figure 14 shows Conversion Time versus Clock Rate Control voltage and Figure 6 shows Differential Linearity error versus Conversion time.

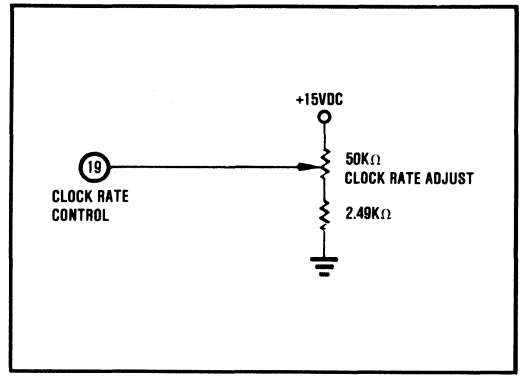


FIGURE 13. Optional Clock Rate Control.

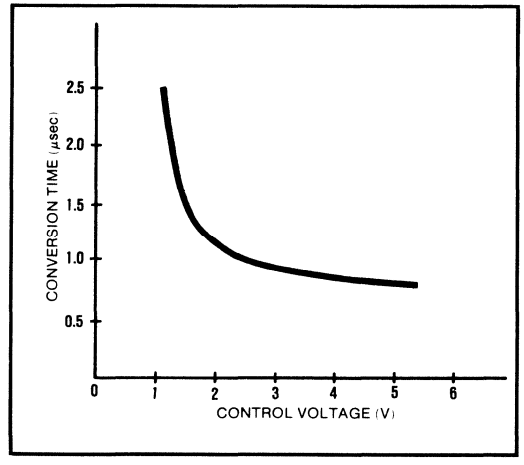


FIGURE 14. Conversion Time versus Clock Rate Control Voltage.

POWER DISSIPATION

The ADC803 dissipates approximately 1.9 watts (typical) and the package has a case-to-ambient thermal resistance (θ_{CA}) of 25°C/W. For operation above +85°C, θ_{CA} should be lowered by a heat sink or by forced air over the surface of the package. See Figure 15 for θ_{CA} requirements above +85°C. Improved thermal contact with the PC card copper ground plane under the case can be achieved using a silicone heat sink compound. On a 0.062" thick PC card with a 16-square inch (minimum) area, this technique will allow operation to +100°C.

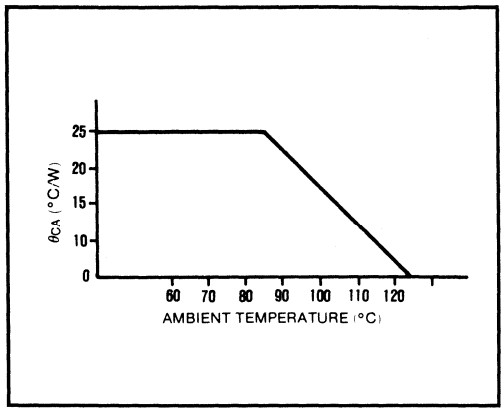


FIGURE 15. θ_{CA} Requirement Above +85°C.

EXTERNAL SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the ADC803 can be shortened with the addition of two external components as shown in Figure 16. This circuit will create a shortened status signal directly proportional to the reduction of resolution. For n bits of resolution, the n+1 bit is used to create the falling edge of the shortened status signal. It is possible to obtain the equivalent of a 10-bit converter with 670nsec conversion time and an 8-bit converter with 500nsec conversion time using this short cycle technique and the external clock rate control shown in Figure 13. To begin a new conversion, simply give the converter a new convert command pulse. The SAR will reset and a new conversion will begin.

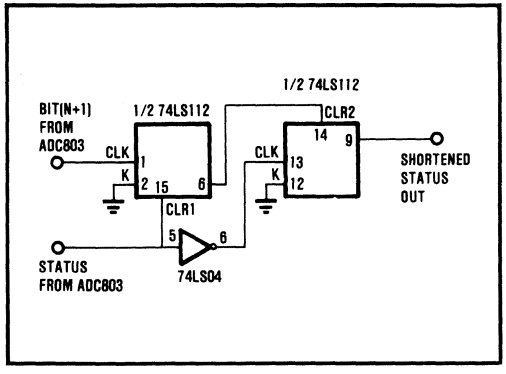


FIGURE 16. External Short Cycle Circuit.

TESTING OF THE ADC803

In order to validate the test results of the ADC803 obtained during final test, the customer must take extreme care in the design and layout of his test fixtures. Proper grounding, correct routing of analog and digital signals and power supply bypassing are crucial in achieving successful results.

ANALOG GROUND, DIGITAL GROUND, SENSE

Figure 17 shows a simplified model of the ADC depicting proper analog and digital grounding. Several analog and digital ground pins have been provided to allow for optimizing the internal layout of the ADC. As will be explained in more detail later, analog and digital grounds should be connected together only at one point by an extremely low resistive and inductive connection (a ground plane is ideal). A special analog ground called "sense" has been provided to eliminate the voltage drop that would otherwise be in the ground return of the R-2R ladder. Measuring the input signal with respect to the sense terminal makes the measurement independent of the impedance that is developed in the connection between the sense terminal and the analog ground, pin 28.

ANALOG-TO-DIGITAL CONVERTER TEST TECHNIQUE

A very effective way of determining the DC performance of an ADC is by using the "servo loop method." The block diagram of this technique is shown in Figure 18. This measurement system automatically locates the analog voltage that causes the digital output to alternate between the desired code and the adjacent code. The computer is programmed to place the desired code on the I/O bus which is one set of inputs to the digital comparator. The other set of inputs to this comparator is the digital output of the ADC. Depending upon the result of this comparison, the integrator is directed to change its output until an equilibrium state is achieved. Once in equilibrium, the DVM measures the analog input to the ADC and transmits the information to the computer via the IEEE-488 bus. The test program checks all the desired code combinations, verifying the performance of the ADC. Test time will range from 10 seconds to several minutes depending on the speed of the test program, settling time of the DVM, and number of codes to be checked.

GROUND LOOPS

Figure 19 illustrates the interaction that occurs between the analog and digital grounds when an ADC is connected into a test circuit. This interaction is created by ground loops. The circuit in Figure 19 shows how ground loops are created when the ADC tester combines digital and analog portions of the circuit together—in this case, the test signal generator (analog) and the digital circuitry that detects the ADC code which corresponds to the analog signal (digital). The ground loop exists when the digital ground connection between the ADC and the tester is in parallel with the analog grounds that connect the tester with the ADC. When the connection is made in this manner some of the digital current is diverted into the analog signal return, which creates a code-dependent error signal due to the resistance in the analog signal return. This error distorts the linearity measurement and induces hysterisis. The error can be substantially reduced if the analog and digital grounds are isolated from each other in the ADC tester.

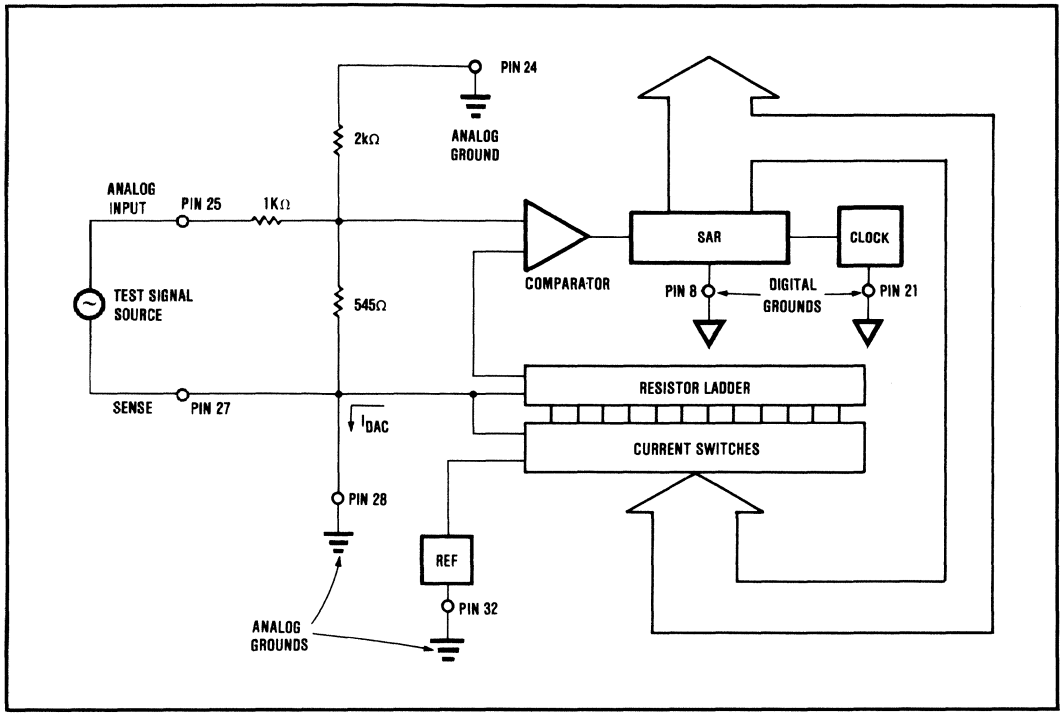


FIGURE 17. Simplified Model of ADC803 Depicting Proper Analog and Digital Ground.

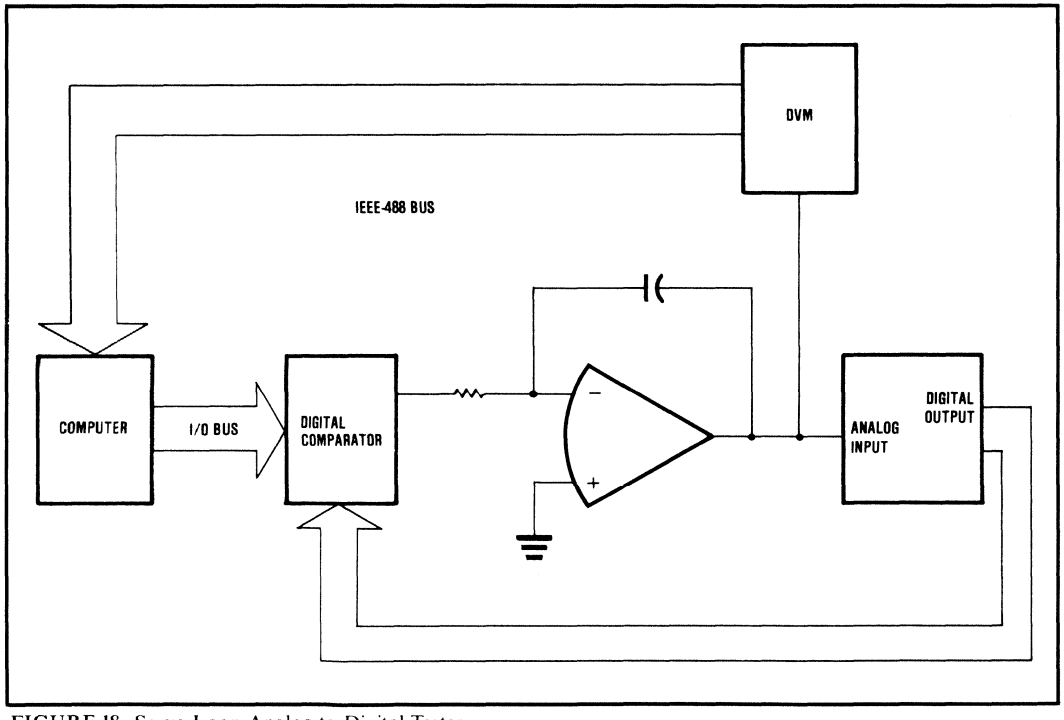


FIGURE 18. Servo Loop Analog-to-Digital Tester.

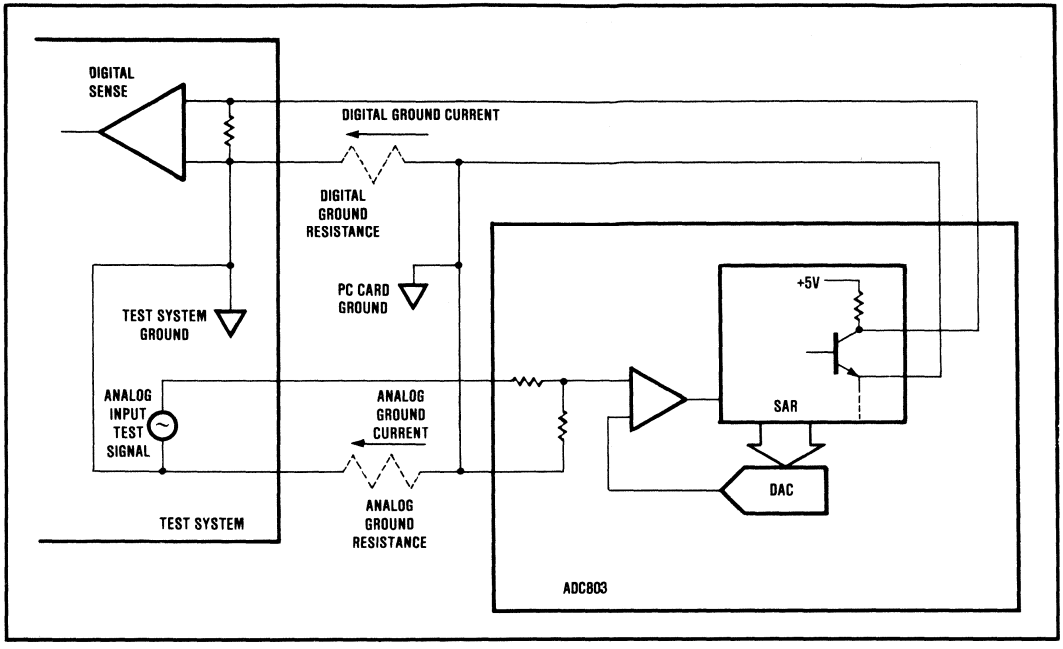


FIGURE 19. Ground Loop Interaction Between Analog and Digital Grounds When ADC Is Connected Into Test Circuit.

BEAT FREQUENCY TEST

A "beat frequency test" applied to an ADC803 with a companion sample/hold illustrates both an effective means of testing the high frequency performance of such a system and demonstrating that the ADC803 with its associated sample/hold is capable of digitizing high frequency signals cleanly. A sample/hold must be used when performing this test to hold the input of the ADC803 constant during the conversion time. Figure 20 is a block diagram of the beat frequency test set up.

The beat frequency test is useful for being able to rapidly determine whether there are any serious problems with the ADC. In this test the input frequency is set at slightly less than one-half the sampling rate. The slight difference is selected to allow the sample point to vary by 1LSB, or less, on successive samples. The data is clocked into a low frequency reconstruction DAC at one-half the sampling rate to enable viewing on an oscilloscope. Figure 21 is a photograph of the response to a full scale input sine wave centered around the MSB and Figure 22 is a photograph of the response of a small signal sine wave centered around the MSB. For comparison, a photograph (Figure 23) is included which shows the response of the ADC803 to a 125Hz input signal which is the same as the beat frequency.

Figure 24 is the PC card layout that was used for the beat frequency test. This layout demonstrates some of the layout practices that must be followed when using a high speed ADC like the ADC803.

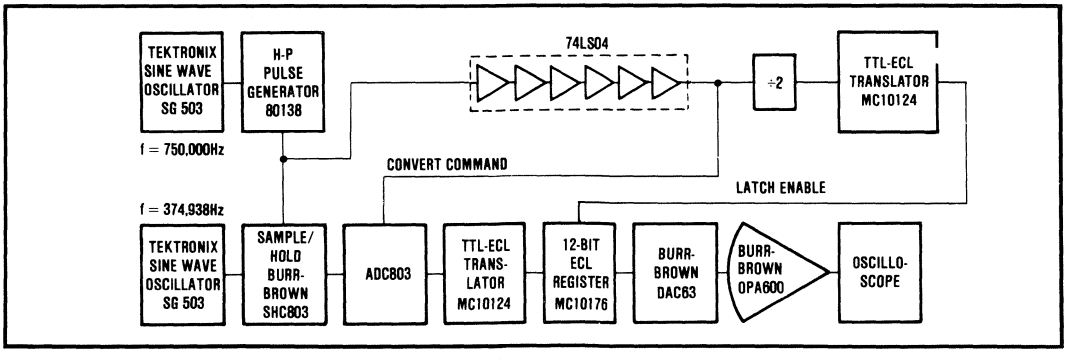


FIGURE 20. Block Diagram of Beat Frequency Test Circuit.

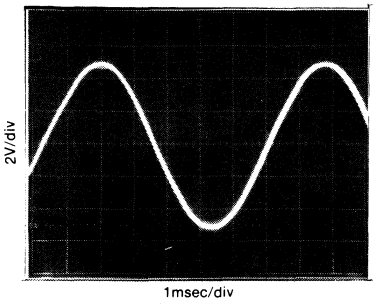


FIGURE 21. Beat Frequency Test Response of Full Scale Sine Wave Input.

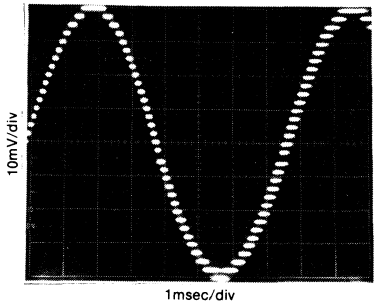


FIGURE 22. Beat Frequency Test Response of Small Signal Sine Wave Input.

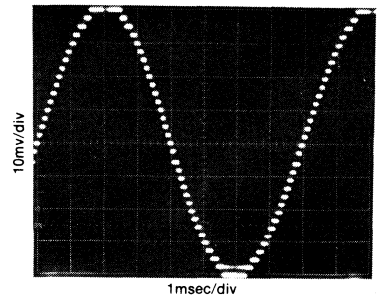
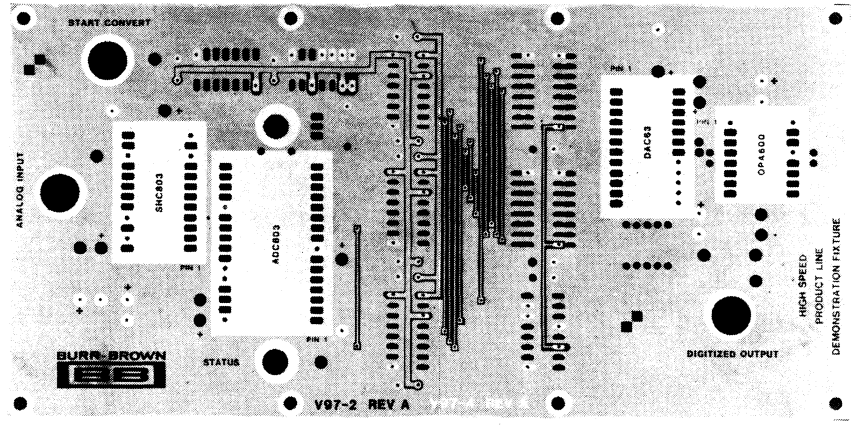
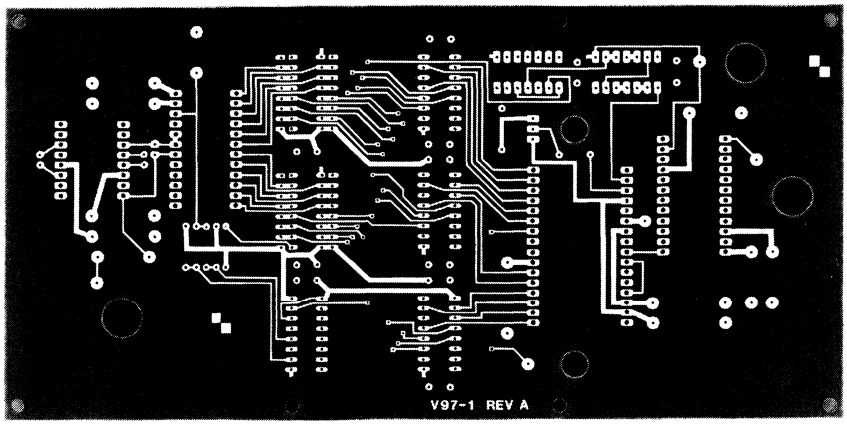


FIGURE 23. Response of Small Signal 125Hz Sine Wave Input.



(a) Top View



(b) Bottom View

FIGURE 24. PC Board Layout for Beat Frequency Test Fixture.

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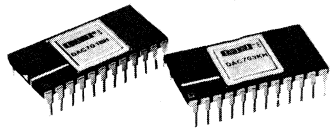


DAC701
DAC703

Monolithic
16-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- MONOLITHIC (1 CHIP) CONSTRUCTION
- OUTPUT AMPLIFIER AND VOLTAGE REFERENCE ON THE CHIP
- VERY ACCURATE: ±0.003% max linearity error
  ±0.006% max diff linearity error
- MONOTONIC OVER FULL SPEC TEMPERATURE RANGE
- PIN-COMPATIBLE TO DAC70, DAC71, DAC72

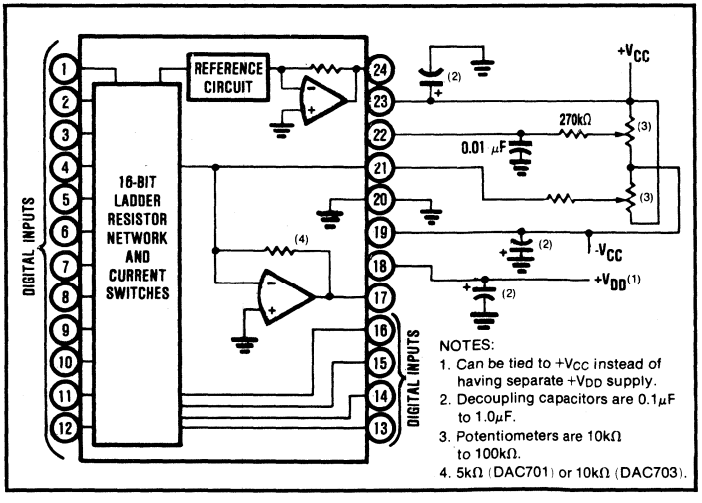
DESCRIPTION

This is another industry first from Burr-Brown–a complete 16-bit D/A converter that includes a precision buried zener voltage reference and a low noise, fast settling output operational amplifier for true voltage output, all on one small monolithic chip. A combination of current switch design techniques accomplishes not only monotonicity over the entire specified temperature range (to 14 bits) but also a maximum endpoint linearity error of ±0.003%. Total full scale drift is limited to ±15ppm/°C maximum (BH grade).

Digital inputs are binary coded and are TTL, LSTTL, 54/74C, and 54/74HC compatible over the entire temperature range. Outputs are 0 to +10V (DAC701) or ±10V (DAC703).

Pin-compatible with the voltage-output DAC71 and DAC72 model families, these D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.

CONNECTION DIAGRAM



PIN ASSIGNMENTS

PIN #	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13	BIT 13
14	BIT 14
15	BIT 15
16	BIT 16 (LSB)
17	V_{OUT}
18	$+V_{DD}$
19	$-V_{CC}$
20	COMMON
21	ZERO ADJUST
22	GAIN ADJUST
23	$+V_{CC}$
24	+6.3V REFERENCE OUTPUT

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies unless otherwise noted.

	DAC701/703KH			DAC701/703BH			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT							
DIGITAL INPUT							
Resolution		16			*		Bits
Logic Levels (TTL/CMOS Compatible)(1)							
Voltage: Logic 1	+2.4		+V_{CC}	*		*	VDC
Logic 0	-1.0		+0.8	*		*	VDC
Current: Logic 1 (V_{IN} = +2.7V)			+40			*	µA
Logic 0 (V_{IN} = +0.4V)		-0.35	-0.5		*	*	mA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error at +25°C		±0.0015	±0.003		*	*	% of FSR(2)
Differential Linearity Error		±0.003	±0.006		*	*	% of FSR
Differential Linearity Error at Bipolar Zero (DAC703)		±0.003	±0.006		±0.0015	±0.003	% of FSR
Gain Error(3)		±0.07	±0.15		±0.05	±0.10	%
Zero Error(3)(4)		±0.05	±0.10		*	*	% of FSR
Monotonicity Temp. Range (14 Bits)	0		+70	-25		+85	°C
DRIFT (over the specification temp. range)							
Total Full Scale Drift							
DAC701		±10	±28		±8.5	±18	ppm of FSR/°C
DAC703		±10	±25		±7	±15	ppm of FSR/°C
Total Error over Temp. Range(5)		±0.08	±0.15		±0.05	±0.10	% of FSR
Gain		±10	±25		±7	±15	ppm/°C
Zero Error Drift(4)							
DAC701		±1.5	±3		*	*	ppm of FSR/°C
DAC703		±4	±10		*	*	ppm of FSR/°C
Differential Linearity over Temp.			+0.009 -0.006			*	% of FSR
Linearity Error over Temp.			±0.006			*	% of FSR
SETTLING TIME (to ± 0.003% of FSR)(6)							
Output: Full Scale Step (2kΩ Load)		4	8		*	*	µsec
1LSB Step (2kΩ Load, at Worst Case Code)		2.5	4		*	*	µsec
Slew Rate (2kΩ Load)		10			*		
OUTPUT							
VOLTAGE OUTPUT							
DAC701		0 to +10			*		V
DAC703		±10			*		V
Output Current	±5			*			mA
Output Impedance (DC)		0.15			*		Ω
Short Circuit to Common Duration		Indefinite			*		
REFERENCE VOLTAGE	+6.0	+6.3	+6.6	+6.24	+6.30	+6.36	V
Source Current Available for External Loads	1.5	2.5		*	*		mA
Temperature Coefficient		±10	±25		*	±15	ppm/°C
Short Circuit to Common Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
±V_{CC} Voltage (No Load)	±13.5	±15.0	±16.5	*	*	*	V
Current		+16/-18	±30		*	*	mA
+V_{DD}(7) Voltage (No Load)	+4.5	+5.0	+16.5	*	*	*	V
Current		+4	+8		*	*	mA
Power Dissipation (V_{DD} = +5V)(7)		530	790		*	*	mW
POWER SUPPLY REJECTION							
±V_{CC}		±0.003	±0.006		±0.0015	±0.003	% of FSR/%ΔV
+V_{DD}		±0.0005	±0.001		*	*	% of FSR/%ΔV
TEMPERATURE RANGE							
Specification	0		+70	-25		+85	°C
Storage	-60		+150	*		*	°C

*Specification same as for DAC701/703KH.

NOTES:

1. Digital inputs are TTL, LSTTL, 54/74C, and 54/74HC compatible over the operating voltage range of V_{DD},+5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD}, +5V to +15V. As logic "0" and logic "1" inputs vary over their specified voltage ranges, the change in the DAC output voltage will not exceed ±0.003% of FSR for BH grade and ±0.006% of FSR for KH grade.
2. FSR means Full Scale Range and is 20V for ±10V range (DAC703) and is 10V for 0 to +10V range (DAC701).
3. Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point.
4. Error at input code $FFFF_H$ for DAC701, $7FFF_H$ for DAC703.
5. With gain and zero errors adjusted to zero at +25°C.
6. Maximum represents the 3σ limit. Not 100% tested for this parameter.
7. Power dissipation is an additional 40mW when V_{DD} is operated at ≥+15V.

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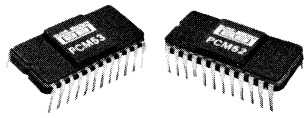


PCM52JG-V
PCM53JG-V

DESIGNED FOR AUDIO

ADVANCE INFORMATION
Subject to Change

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTER

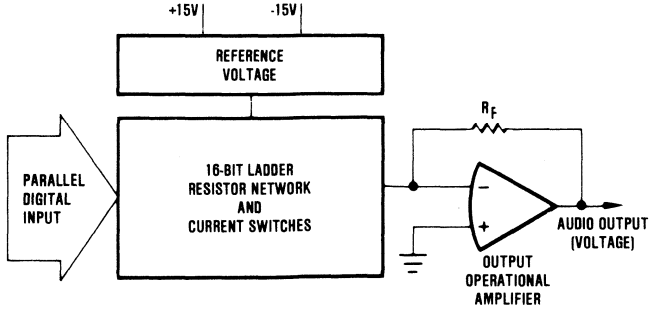
FEATURES

- LOW COST
- NO EXTERNAL COMPONENTS REQUIRED
- 16-BIT RESOLUTION
- 16-BIT MONOTONICITY, typ
- 0.001% OF FSR TYP DIFFERENTIAL LINEARITY ERROR
- 0.002% THD (FS Input, 16 Bits), typ
- 0.02% THD (-20dB, 16 Bits), typ
- 3μsec SETTLING TIME, typ
- 96dB DYNAMIC RANGE
- ±10V (PCM53) AND ±5V (PCM52) AUDIO OUTPUT AVAILABLE
- EIAJ STC-007 COMPATIBLE
- INDUSTRY-STANDARD PIN OUT
- COMPACT, 24-PIN, DIL PACKAGE

DESCRIPTION

The PCM52JG-V and PCM53JG-V are state-of-the-art, fully monolithic, digital-to-analog converters that are designed and specified for digital audio applications. These devices employ a segmented architecture and ultra-stable, nichrome (NiCr), thin-film, well-matched resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature range.

The PCM52JG-V and PCM53JG-V are completely self-contained with stable, low noise, internal, zener voltage reference; high speed current switches; resistor ladder network; and fast-settling, low noise, output operational amplifier all on a single monolithic chip. A special, open-loop reference circuit helps provide the fast-settling time required for critical audio applications. The converters can be operated using two power supplies (±15V) instead of three separate supplies. Few external components are necessary for operation, and all critical specifications are 100% tested. This helps to assure the user of high system reliability and outstanding overall system performance.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C rated power supplies unless otherwise noted.

MODEL	PCM52JG-V/PCM53JG-V MIN	TYP	MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL/CMOS Compatible)				
Logic "1" at +40µA	+2.4		+V_{CC}	VDC
Logic "0" at -0.5mA	0		+0.8	VDC
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error		±0.1	±1.0	%
Bipolar Zero Error(1)		±10	±50	mV
Differential Linearity Error at Bipolar Zero		0.001	0.005	% of FSR(2)
Noise (rms) (20Hz to 20kHz) at Bipolar Zero				
PCM52JG-V(3)		15	30	µV
PCM53JG-V(3)		30	60	µV
TOTAL HARMONIC DISTORTION(4)				
16-Bit Resolution				
V_O = ±FS at f = 420Hz		0.002	0.004	%
V_O = -20dB at f = 420Hz		0.02	0.04	%
V_O = -60dB at f = 420Hz		1.9	4.0	%
MONOTONICITY		16		Bits
DRIFT (0°C to +70°C)				
Total Bipolar Drift		±25	±150	ppm of FSR/°C
(includes gain, offset, and linearity drift)		±0.1	±0.68	% of FSR
		±0.01	±0.06	dB
Bipolar Zero Drift		±4	±20	ppm of FSR/°C
SETTLING TIME (To ±0.006% of FSR)				
Output: 10V Step		3		µsec
1LSB Step		1		µsec
Deglitcher Delay (THD Test)(5)		2.5	4.0	µsec
Slew Rate		10		V/µsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Ranges, PCM53JG-V	±9.8	±10	±10.2	V
PCM52JG-V	±4.9	±5	±5.1	V
Output Current	±5			mA
Output Impedance (DC)		0.1		Ω
Short-Circuit Duration	Indefinite to Common			
POWER SUPPLY				
SENSITIVITY				
+V_{CC}		±0.001		% of FSR/%V_S
-V_{CC}		±0.001		% of FSR/%V_S
+V_{DD}		±0.001		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS				
Voltage, ±V_{CC}(6)	±14.25	±15	±15.75	VDC
+V_{DD}(6)	+4.75	+5	+15.75	VDC
(+V_{DD} may be connected to +V_{CC} supply voltage. Result is slightly increased total power dissipation of approximately 40mW).				
Supply Drain +V_{CC}(6)		+18	+25	mA
(no load) -V_{CC}(6)		-18	-25	mA
+V_{DD}(6)		+4	+10	mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	-25		+85	°C

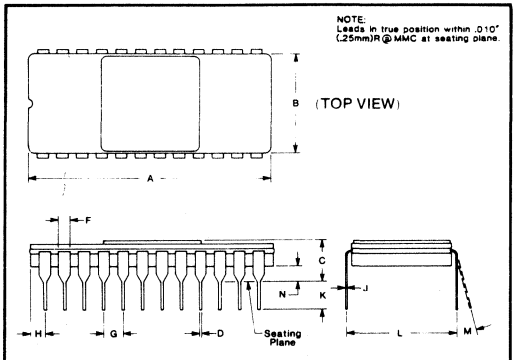
NOTES:

1. Adjustable to zero with external potentiometer.
2. FSR means Full Scale Range and is 20V for ±10V (PCM53JG-V) and 10V for ±5V range (PCM52JG-V).
3. Characterization units show at least two sigma units to meet this specification. Not 100% final tested.
4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 2. Burr-Brown may calculate THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion", but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated.
5. Deglitcher or Sample/Hold delay used in THD measurement test circuit. See Figures 2 and 3.
6. See Connection Diagram and Pin Assignments.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltages	±18VDC
Input Logic Voltage	-1V to +Supply Voltage
Storage Temperature	-55°C to +100°C
Lead Temperature	
During Soldering	10sec at +300°C

MECHANICAL



NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

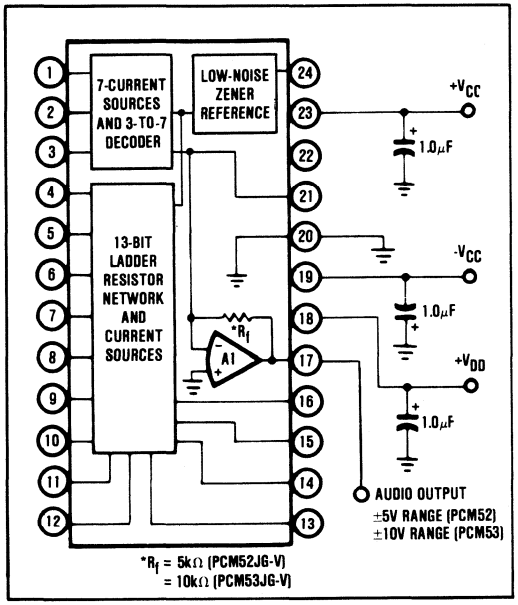
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.237	1.263	31.42	32.08
B	.514	.526	13.06	13.36
C	.178	.230	4.52	5.84
D	.016	.020	0.41	0.51
F	.050	.070	1.27	1.78
G	.100 BASIC		2.54 BASIC	
H	.065	.085	1.65	2.16
J	.008	.012	0.20	0.30
K	.100	.200	2.54	5.08
L	.600 BASIC		15.24 BASIC	
M	—	15°	—	15°
N	.035	.055	0.89	1.40

Actual package, such as cover appearance, may vary slightly from unit to unit. Pin spacing will not change.

PIN ASSIGNMENTS

Pin No.	PCM52/53JG-V		
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16 (LSB)
5	Bit 5	17	±5V AUDIO OUT (PCM52JG-V) ±10V AUDIO OUT (PCM53JG-V)
6	Bit 6	18	$+V_{DD}$
7	Bit 7	19	$-V_{CC}$
8	Bit 8	20	COMMON
9	Bit 9	21	SUMMING JUNCTION
10	Bit 10	22	TEST POINT
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	REFERENCE OUT (+6.3V)

CONNECTION DIAGRAM



THEORY OF OPERATION AND AUDIO SPECIFICATIONS

The transfer function of an ideal binary D/A converter is a set of discrete output levels that lie on a straight line as shown in Figure 1. The number of possible discrete output levels, or resolution, is equal to 2^n where n is the number of digital inputs or "bits". The PCM52/53 has 2^{16} or 65,536 possible output levels. Another method of expressing resolution that is useful in audio applications is Dynamic Range.

DYNAMIC RANGE

The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, or about 96dB for a 16-bit converter. The actual, or useful, Dynamic Range is limited by noise and linearity

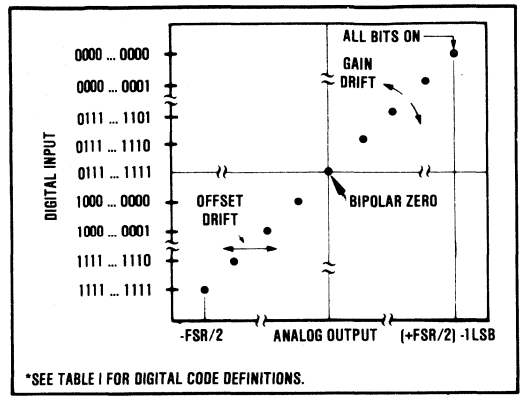


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is Total Harmonic Distortion (THD).

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error in unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM52/53 is shown in Figure 2. A timing diagram for the control logic is shown in Figure 3.

If we assume that the error due to the test circuit is negligible, then the rms value of the PCM52/53 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2} \qquad (1)$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM52/53 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \frac{\epsilon_{rms}}{E_{rms}} = \frac{\sqrt{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

where E_{rms} is the rms signal-voltage level.

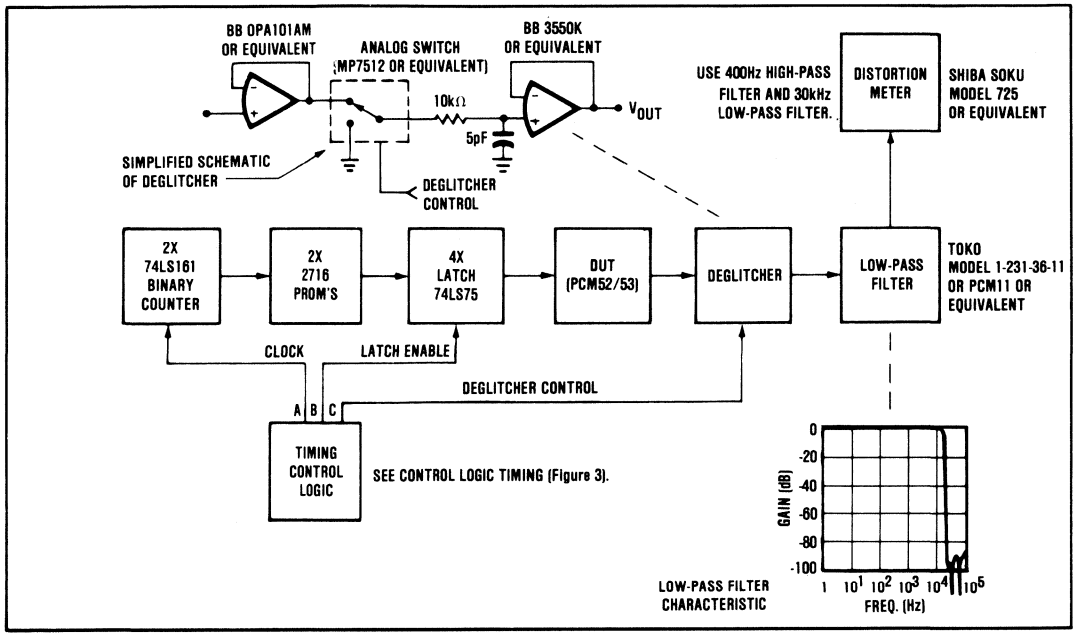


FIGURE 2. Block Diagram of Distortion Test Circuit.

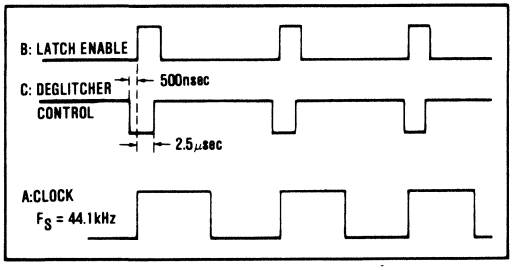


FIGURE 3. Control Logic Timing for PCM52/53 Distortion Test Circuit.

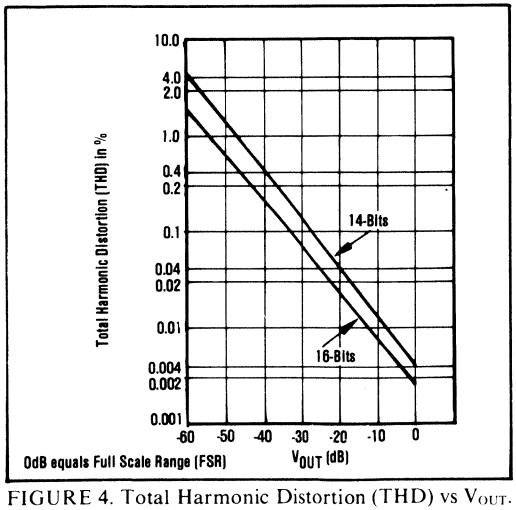


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

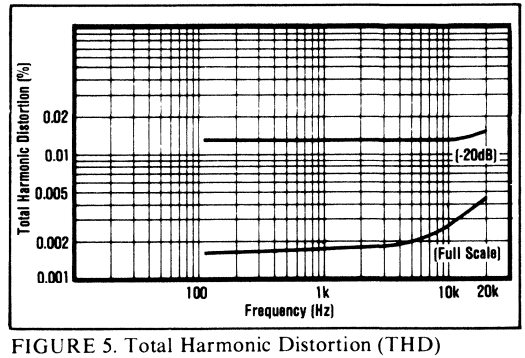


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

This expression indicates that, in general there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM52/53 the test period was chosen to be 22.7μsec (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, -20dB, and -60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

DIGITAL INPUT CODES

The PCM52/53 accepts complementary digital input codes in binary format. It may be connected by the user

for either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
		COB	CTC*
	MSB LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

DISCUSSION OF SPECIFICATIONS

The PCM52/53 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are Total Harmonic Distortion, Differential Linearity Error, Bipolar Zero Error, parameter shifts with time and temperature, and settling time effects on accuracy. The PCM52/53 is factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and Offset drift shifts the line left or right over the operating temperature range. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is the deviation from zero volts out and is factory-trimmed to typically ±10mV at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 7.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at Bipolar Zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM52/53 is factory-trimmed to typically ±0.001% of FSR.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the Offset and Gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM52/53 is designed so that these drifts are in opposite directions so that the Bipolar Zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM52/53 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM52/53 power supply sensitivity is specified for ±0.001% of FSR/%V_{CC} for all supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 6).

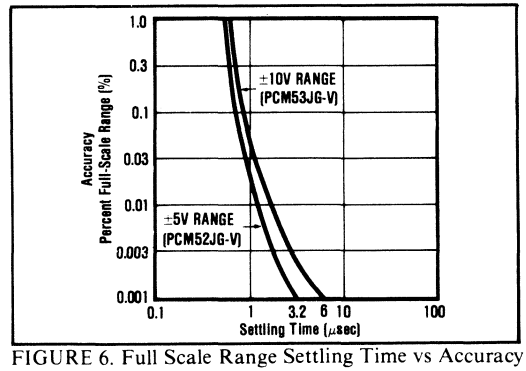


FIGURE 6. Full Scale Range Settling Time vs Accuracy.

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power

supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM52/53.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the Bipolar Zero Error (offset) may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 7.

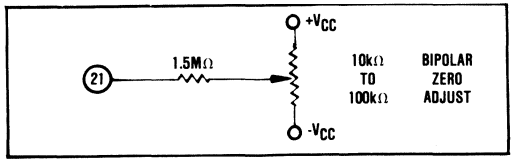


FIGURE 7. Optional External Bipolar Zero Adjust.

The potentiometer should have adequate resolution, at least 10 turns for full-scale resistance.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM52/53 to prevent noise pickup. Refer to Figure 8 for the relationship of Bipolar Zero adjust on the D/A converter transfer function.

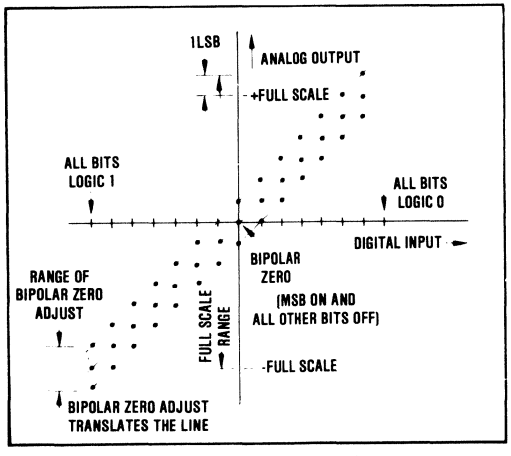


FIGURE 8. Effect of Bipolar Zero Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the bipolar zero potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V and ±5V output ranges.

INSTALLATION CONSIDERATIONS

If 14-bit resolution is desired, bit 15 (pin 15) and bit 16 (pin 16) should be connected to $+V_{DD}$ through a 1kΩ resistor to insure that these bits remain off.

Figure 9 shows the connection diagram for a PCM52/53.

TABLE II. Digital Input and Analog Output Relationship.

DIGITAL INPUT CODE	OUTPUT VOLTAGE	
	16-Bit Resolution	14-Bit Resolution
Complementary Bipolar Offset Binary (COB) ±10V (PCM53JG-V)		
One LSB	+305μV	+1.22mV
All Bits On 00 .. 00	+9.99969V	+9.99878V
All Bits Off 11 .. 11	-10.0000V	-10.0000V
±5V (PCM52JG-V)		
One LSB	+152μV	+610μV
All Bits On 00 .. 00	+4.999848V	+4.99939V
All Bits Off 11 .. 11	-5.0000V	-5.0000V

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. R_L should be located as close

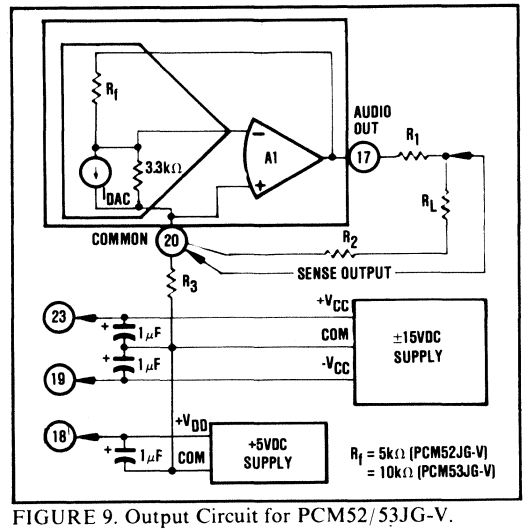


FIGURE 9. Output Circuit for PCM52/53JG-V.

as possible to the PCM52/53 for optimum performance.

The PCM52/53 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

The PCM52/53 is not normally sensitive to electrostatic discharge (ESD).

APPLICATIONS

Figures 10 and 11 show a circuit diagram and timing diagram of a single PCM52/53 used to obtain both left and right channel audio output in a typical digital audio system. The Sony CX-7934 and associated LSI logic contain all of the required circuitry for error detection, correction, and formatting of the digital data obtained from the Compact Disc prior to sending this information to the D/A converter. The CX-7934 is used in a parallel output mode where the left and right channel parallel data are time-shared. Since the digital inputs of the PCM52/53 are TTL-compatible, they can be connected directly to the parallel outputs of the CX-7934. Only a single inverter is required (Bit 1) to convert the two's complement output code of the CX-7934 to offset binary. The audio output of the PCM52/53 is alternately time-shared between the left and right channels. The design is greatly simplified because the PCM52/53 is a complete D/A converter.

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 12. The S/H amplifier for the

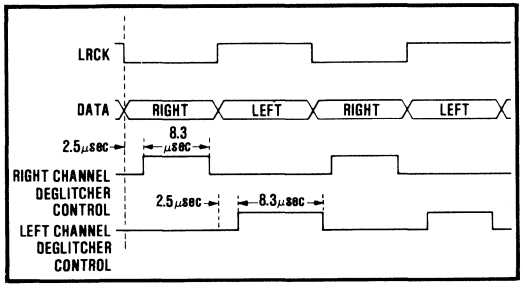


FIGURE 11. Timing Diagram for the Digital Audio System using PCM52/53 and Sony LSI Logic.

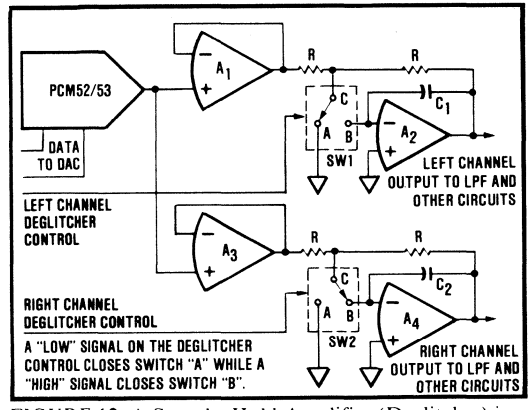


FIGURE 12. A Sample/Hold Amplifier (Deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.

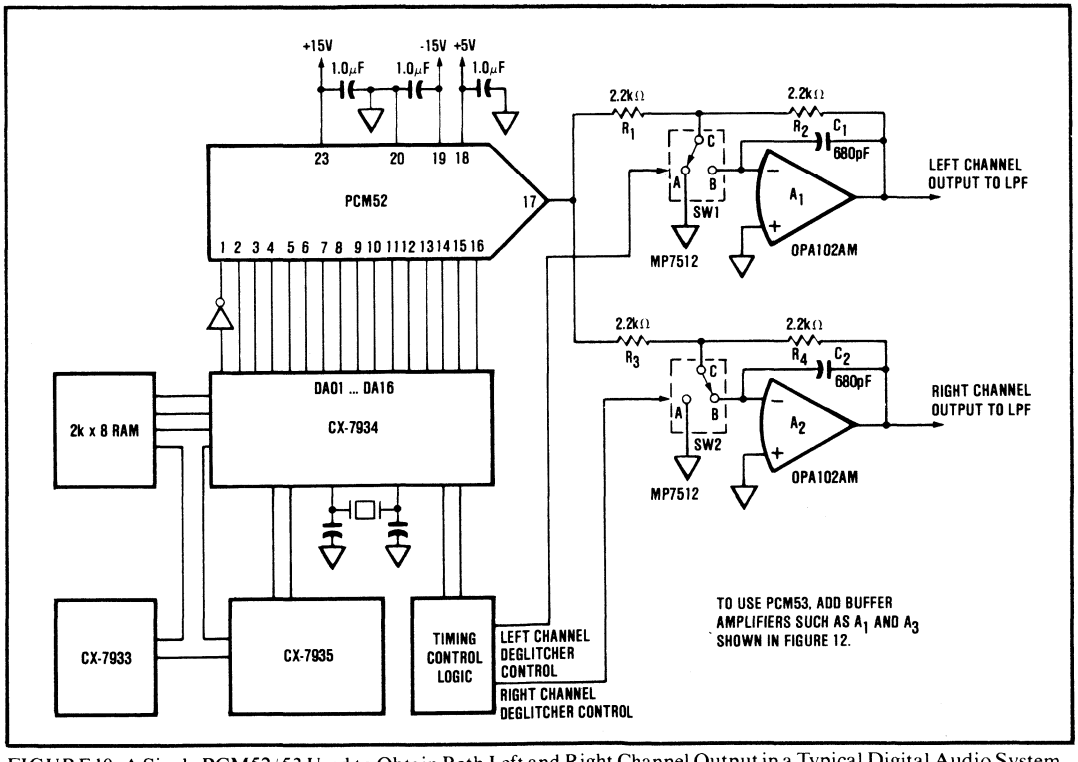


FIGURE 10. A Single PCM52/53 Used to Obtain Both Left and Right Channel Output in a Typical Digital Audio System.

left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the sample mode, there is no increase in distortion caused by the modulation effect of R_{on} by the audio signal.

Figure 13 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5μsec (tω) is provided to eliminate the glitch and allow the output of the PCM52/53 to settle within a small error band around its final value before connecting it to the channel output.

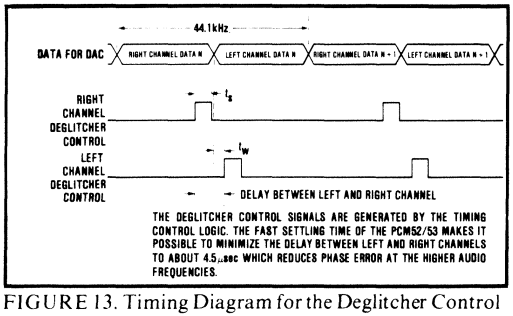


FIGURE 13. Timing Diagram for the Deglitcher Control Signals.

Due to the fast settling time of the PCM52/53, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very-high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music. One method of avoiding this problem and obtaining a linear phase response is to use an oversampling digital filter technique as shown in Figure 14. Figure 15 is the timing diagram for this technique. This circuit requires a very fast D/A converter since the sampling frequency is multiplied by a factor of two or more. This technique results in intermodulation products being created, by mixing the sampling frequency and components of the audio frequency, that are far outside the audio band of 0 to 20kHz. These unwanted frequencies are easily removed by a low-order linear-phase analog filter following the deglitcher circuit since a sharp amplitude response is not required. A single PCM52/53 can be used for both the left and right channel as long as the oversampling rate of the digital filter is two. An oversampling rate of four can be used if a separate PCM52/53 is used for each channel. This would reduce the complexities of the analog filter required even further (at the expense of an additional D/A converter).

Another factor to consider when choosing a D/A converter for digital audio applications is that the linearity of the total harmonic distortion versus output signal should be good since a change in the background noise level can be audible. The design of the PCM52/53 ensures that the linearity of the total harmonic distortion versus output signal level is very good over the full range of amplitude and frequencies. Also, no special grounding or shielding techniques are required to obtain good signal-to-noise ratio with the PCM52/53. Some converters require a high frequency clock which can couple to the analog output of the D/A converter through the output wiring and ground circuitry.

The PCM52 and PCM53 D/A converters provide a complete solution to one of the most critical portions of a digital audio system. Since the sound of the system can be affected by the D/A converter more than any other single component, the selection of which converter to use should be made with care.

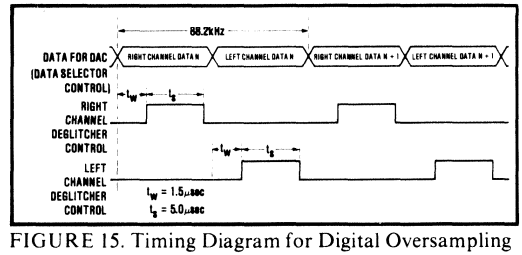


FIGURE 15. Timing Diagram for Digital Oversampling Technique when the Sampling Frequency is Multiplied by a Factor of Two.

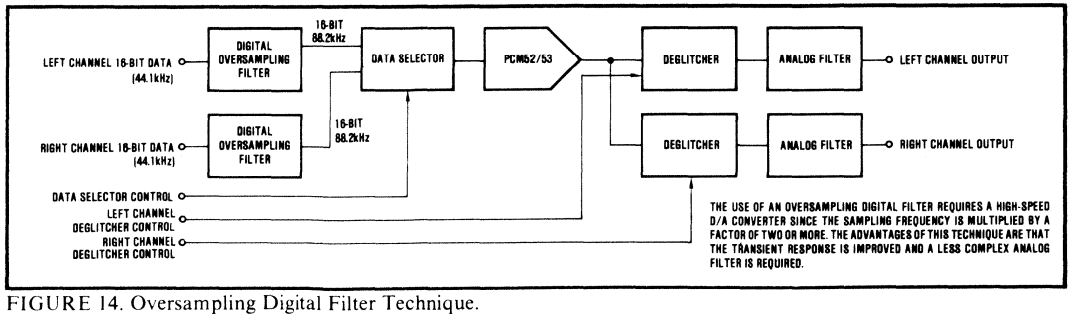


FIGURE 14. Oversampling Digital Filter Technique.

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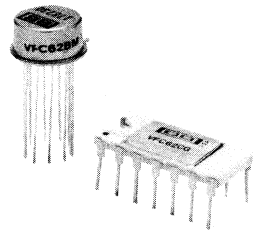


VFC62

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE
- ACTIVE PULL-UP OUTPUT

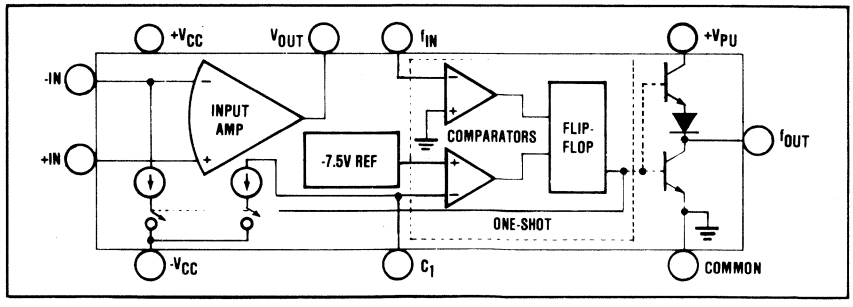
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- 2-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC62 monolithic voltage-to-frequency and frequency-to voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. In the noise-immune digital form the analog signal may be transmitted long distances without degradation. It may be converted to a binary number with a counter or microprocessor or may be returned to analog form using a frequency-to-voltage converter.

The digital output is an active pull-up type which provides better load driving capability than the usual open collector outputs. Output pulses are DTL, TTL and CMOS compatible. High accuracy (±0.005% max nonlinearity at 10kHz) is achieved with relatively few external components. Only one resistor and two capacitors are required.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC62BG/BM/SM MIN	VFC62BG/BM/SM TYP	VFC62BG/BM/SM MAX	VFC62CG/CM MIN	VFC62CG/CM TYP	VFC62CG/CM MAX	UNITS
V/F CONVERTER $f_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2	*		*	V
	Fig. 4 with $e_1 = 0$	< 0		-10	*		*	V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with e_2 + = 0(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.03		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error	Input Offset Voltage(3)			±15			*	ppm of FSR
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)				±5			*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR
Full Scale Drift (offset drift & gain drift(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
ACTIVE PULL-UP OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Voltage, Logic "1"		V_{PU} - 2.6		V_{PU}	*		*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100			*		nsec
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range, V_{CC}		±13		±20	*		*	V
Pull-up Voltage		+3.5		+V_{CC}	*		*	V
Quiescent Current	not including load current		±6	±6.7		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC62BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are 0.01% at 10kHz, 0.2% at 100kHz.
7. Exclusive of external components drift.
8. FSR = Full Scale Range (corresponds to full scale frequency and full scale input voltage).
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

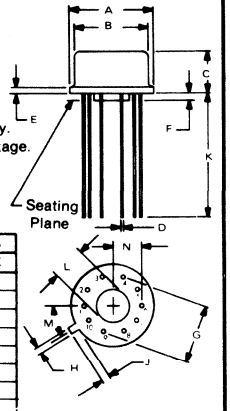
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	±V_{CC}
Input Voltage, +Input	±V_{CC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC62BM, CM/SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

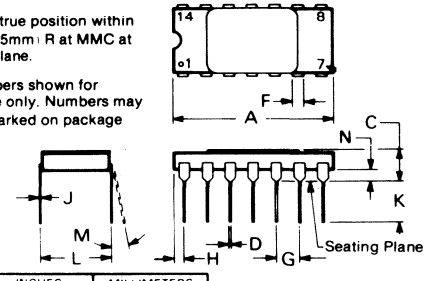


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	--	12.70	--
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC62BG/CG CERAMIC DUAL-IN-LINE

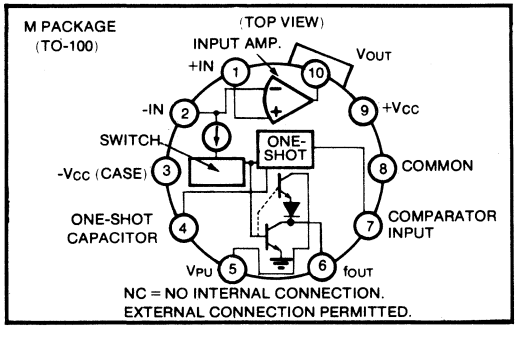
NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

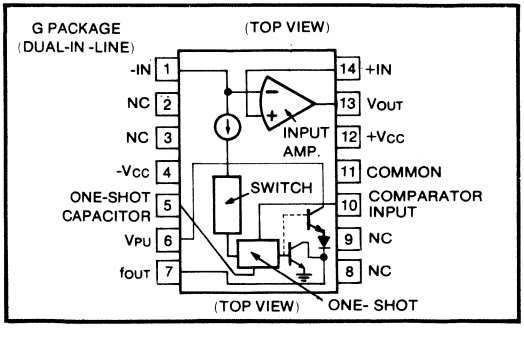
Pin numbers shown for reference only. Numbers may not be marked on package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	670	710	17 02	18 03
C	065	170	1 65	4 32
D	015	021	0 38	0 53
F	045	060	1 14	1 52
G	100 BASIC		2 54 BASIC	
H	025	070	0 64	1 78
J	008	012	0 20	0 30
K	120	240	3 05	6 10
L	300 BASIC		7 62 BASIC	
M		10°		10°
N	009	060	0 23	1 52

PIN CONFIGURATIONS





DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC62 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

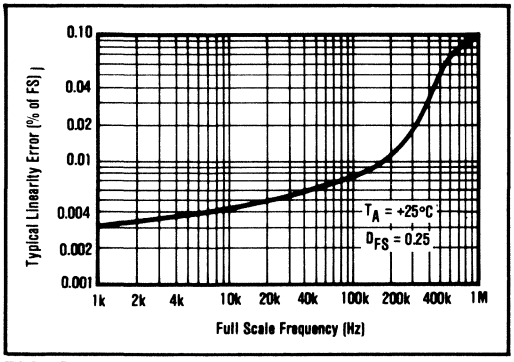


FIGURE 1. Linearity Error vs Full Scale Frequency.

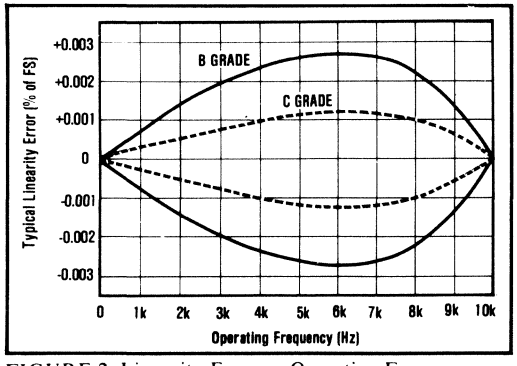


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC62 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC62.

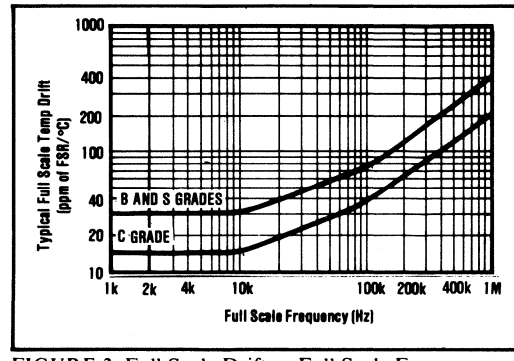


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC62 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC62 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC62 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an active pull-up output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC62 is derived as follows

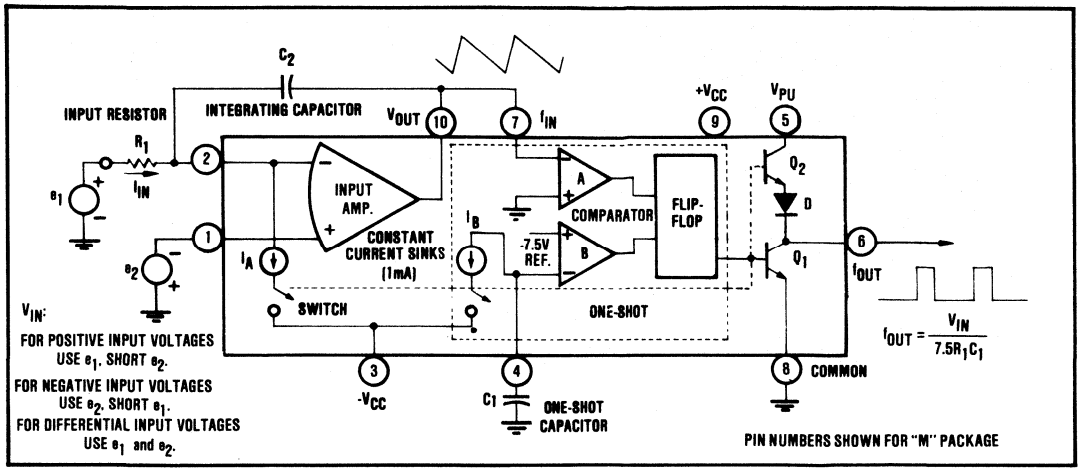


FIGURE 4. Functional Block Diagram of the VFC62.

for the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_1 + t_2$, the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

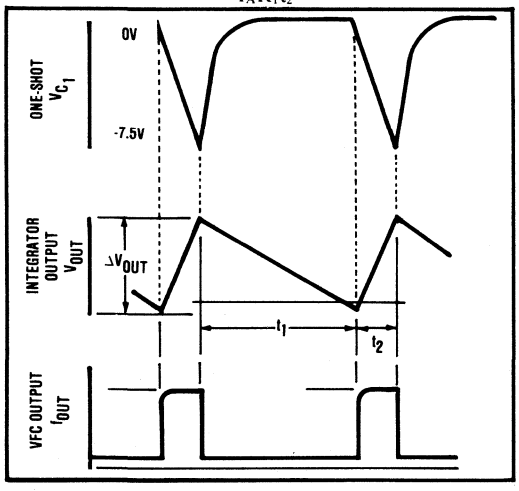


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yields } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

Since $I_A = I_B$ the result is

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC62 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC62, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user-determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

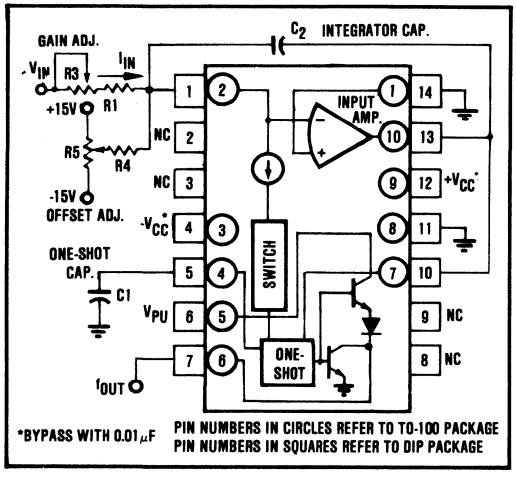


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

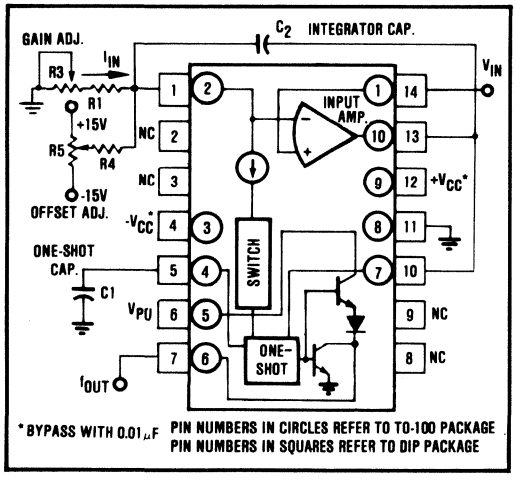


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

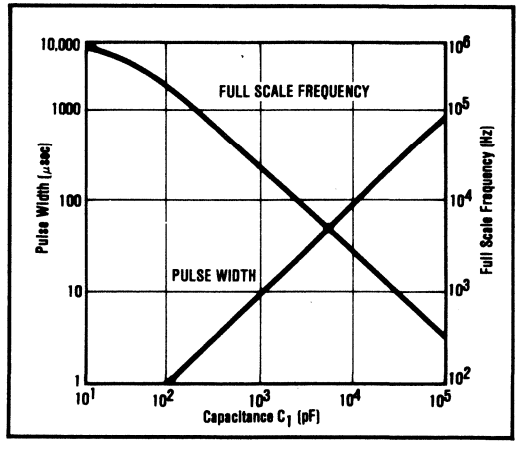


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\ (\mu F) = \begin{cases} \frac{100}{f_{FS}}\ ;\ \text{if } f_{FS} \leq 100\text{kHz} \\ 0.001;\ \text{if } 100\text{kHz} < f_{FS} \leq 500\text{kHz} \\ 0.0005;\ \text{if } f_{FS} > 500\text{kHz} \end{cases} \quad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\qquad$ $[(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100\text{kHz}] - 15$

$= 315\text{pF}$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ \text{max}/0.25\text{mA}$ $\qquad$ $V_{IN}\ \text{max}/0.5\text{mA}$ if $D_{FS} = 0.5$

$= 10\text{V}/0.25\text{mA}$

$= 40\text{k}\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100\text{kHz}$

$= 0.001\mu\text{F}$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

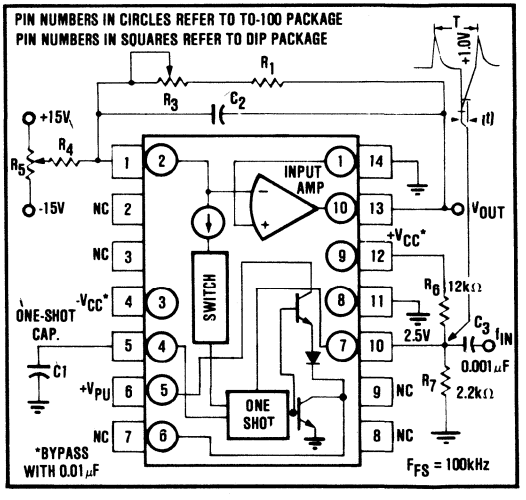


FIGURE 9. Connection Diagram for F/V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

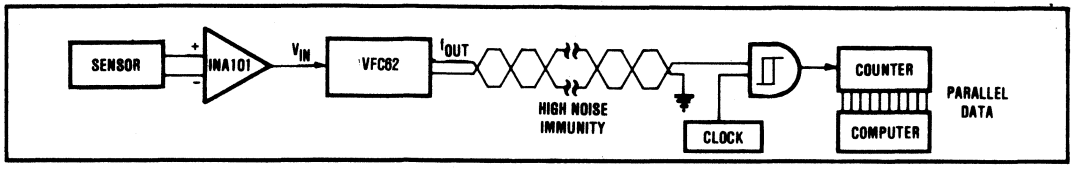


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

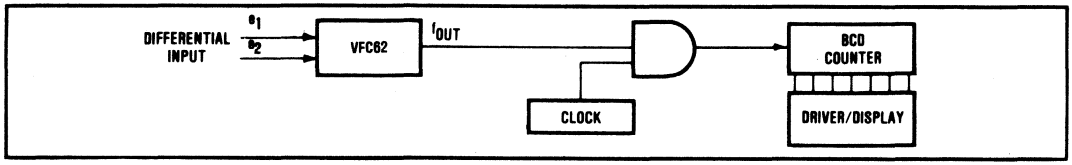


FIGURE 11. Inexpensive Digital Panel Meter.

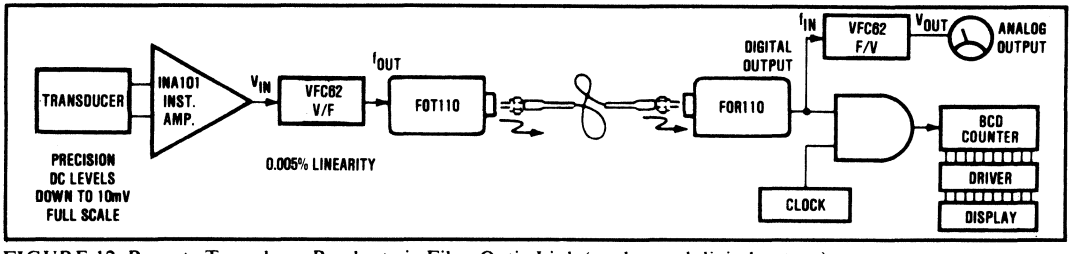


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

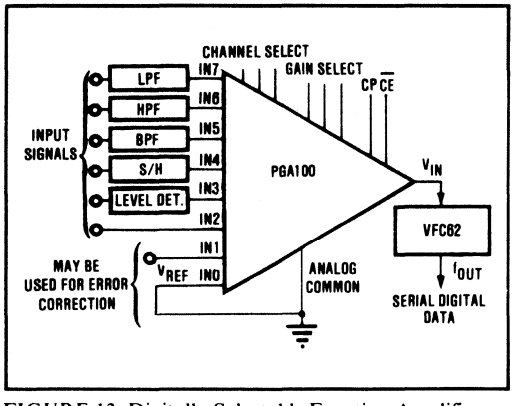


FIGURE 13. Digitally Selectable Function Amplifier with Serial Data Output.

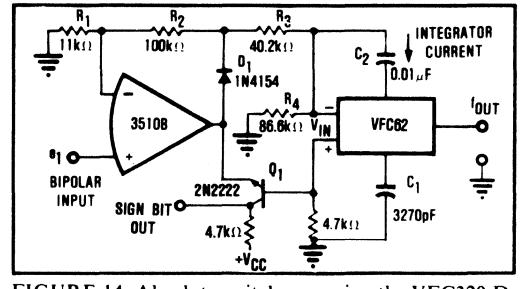


FIGURE 14. Absolute switchover using the VFC320 D_1 and Q_1 switch on alternately as polarity of input signal changes, thus maintaining direction of integrator current. V/F converter cannot distinguish between signal polarities of the same magnitude and so generate the same frequency for both.

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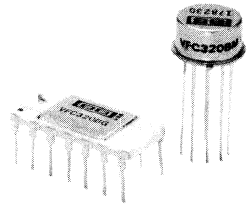


VFC320

Voltage-to-Frequency and Frequency-to-Voltage CONVERTER

FEATURES

- HIGH LINEARITY, 12 to 14 bits
  - ±0.005% max at 10kHz FS
  - ±0.03% max at 100kHz FS
  - ±0.1% typ at 1MHz FS
- V/F OR F/V CONVERSION
- 6-DECADE DYNAMIC RANGE
- 20ppm/°C max GAIN DRIFT
- OUTPUT DTL/TTL/CMOS COMPATIBLE

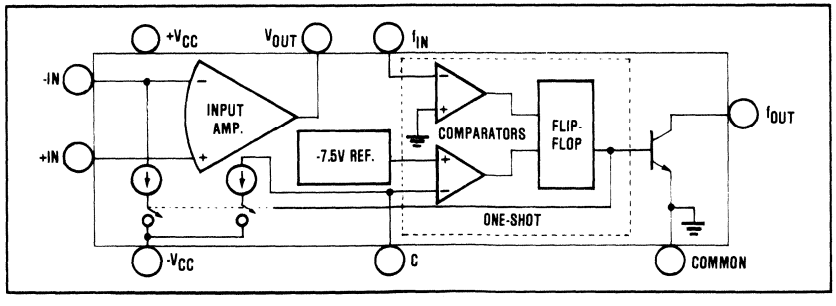
APPLICATIONS

- INEXPENSIVE A/D AND D/A CONVERTER
- DIGITAL PANEL METERS
- TWO-WIRE DIGITAL TRANSMISSION WITH NOISE IMMUNITY
- FM MOD/DEMOD OF TRANSDUCER SIGNALS
- PRECISION LONG TERM INTEGRATOR
- HIGH RESOLUTION OPTICAL LINK FOR ISOLATION
- AC LINE FREQUENCY MONITOR
- MOTOR SPEED MONITOR AND CONTROL

DESCRIPTION

The VFC320 monolithic voltage-to-frequency and frequency-to-voltage converter provides a simple low cost method of converting analog signals into digital pulses. The digital output is an open collector and the digital pulse train repetition rate is proportional to the amplitude of the analog input voltage. Output pulses are compatible with DTL, TTL, and CMOS logic families.

High linearity (0.005%, max at 10kHz FS) is achieved with relatively few external components. Two external resistors and two external capacitors are required to operate. Full scale frequency and input voltage are determined by a resistor in series with -IN and two capacitors (one-shot timing and input amplifier integration). The other resistor is a non-critical open collector pull-up (f_{OUT} to $+V_{CC}$). The VFC320 is available in three performance temperature grades and two package configurations. The TO-100 versions are hermetically sealed, and specified for the -25°C to +85°C and -55°C to +125°C ranges, and the dual-in-line units are specified from -25°C to +85°C.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC power supply unless otherwise noted.

CHARACTERISTICS	CONDITIONS	VFC320BG/BM/SM MIN	VFC320BG/BM/SM TYP	VFC320BG/BM/SM MAX	VFC320CG/CM MIN	VFC320CG/CM TYP	VFC320CG/CM MAX	UNITS
V/F CONVERTER $F_{OUT} = V_{IN}/7.5\ R_1C_1$, Figure 4								
INPUT TO OP AMP								
Voltage Range(1)	Fig. 4 with $e_2 = 0$	> 0		Note 2				V
	Fig. 4 with $e_1 = 0$	< 0		-10				V
Current Range(1)	$I_{IN} = V_{IN}/R_{IN}$	+0.25		+750	*		*	µA
Bias Current								
Inverting Input			4	8		*	*	nA
Noninverting Input			10	30		*	*	nA
Offset Voltage(3)				±0.15			*	mV
Offset Voltage Drift			±5			*		µV/°C
Differential Impedance		300 || 5	650 || 5		*	*		kΩ || pF
Common-mode Impedance		300 || 3	500 || 3		*	*		kΩ || pF
ACCURACY								
Linearity Error(1)(4)(5)	Fig. 4 with $e_2 = 0$(6)							
	0.01Hz ≤ f_{OUT} ≤ 10kHz		±0.004	±0.005		±0.0015	±0.002	% of FSR
	0.1Hz ≤ f_{OUT} ≤ 100kHz		±0.008	±0.030		*	*	% of FSR
	1Hz ≤ f_{OUT} ≤ 1MHz		±0.1			*		% of FSR
Offset Error Input Offset Voltage(3)				±15			*	ppm of FSR/°C
Offset Drift(7)			±0.5			*		ppm of FSR/°C
Gain Error(3)				±5			*	% of FSR
Gain Drift(7)	f = 10kHz			50			20	ppm of FSR
Full Scale Drift (offset drift & gain drift)(7)(8)(9)	f = 10kHz			50			20	ppm of FSR/°C
Power Supply Sensitivity	±V_{CC} = 14VDC to 18VDC			±0.015			*	% of FSR/%
DYNAMIC RESPONSE								
Full Scale Frequency	C_{LOAD} ≤ 50pF			1			*	MHz
Dynamic Range		6			*			decades
Settling Time	(V/F) to specified linearity for a full scale input step		Note 10			*		
Overload Recovery	< 50% overload		Note 10			*		
OPEN COLLECTOR OUTPUT								
Voltage, Logic "0"	I_{SINK} = 8mA, max			0.4			*	V
Leakage Current, Logic "1"	V_O = 15V		0.01	1.0		*	*	µA
Voltage, Logic "1"	External pull-up resistor required (see Figure 4)			V_{PU}			*	V
Duty Cycle at FS	For Best Linearity		25			*		%
Fall Time	I_{OUT} = 5mA, C_{LOAD} = 500pF		100	*		*		nsec
F/V CONVERTER $V_{OUT} = 7.5\ R_1C_1\ F_{IN}$, Figure 9								
INPUT TO COMPARATOR								
Impedance		50 || 10	150 || 10		*	*		kΩ || pF
Logic "1"		+1.0		+V_{CC}	*		*	V
Logic "0"		-V_{CC}		-0.05	*		*	V
Pulse-width Range		0.25			*			µsec
OUTPUT FROM OP AMP								
Voltage	I_O = 7mA	0 to +10			*			V
Current	V_O = 7VDC	+10			*			mA
Impedance	Closed-loop			0.1			*	Ω
Capacitive Load	Without oscillation			100			*	pF
POWER SUPPLY								
Rated Voltage			±15			*		V
Voltage Range		±13		±20	*		*	V
Quiescent Current			±6	±6.7		*	*	mA
TEMPERATURE RANGE								
Specification								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Operating								
B and C Grades				-25 to +85				°C
S Grade				-55 to +125				°C
Storage		-65		+150	-65		+150	°C

*Specification the same as for VFC320BG/BM/SM.

NOTES:
1. A 25% duty cycle at full scale (0.25mA input current) is recommended where possible to achieve best linearity.
2. Determined by R_{IN} and full scale current range constraints.
3. Adjustable to zero. See Offset and Gain Adjustment section.
4. Linearity error at any operating frequency is defined as the deviation from a straight line drawn between the full scale frequency and 0.1% of full scale frequency. See Discussion of Specifications section.
5. When offset and gain errors are nulled, at an operating temperature, the linearity error determines the final accuracy.
6. For $e_1 = 0$ typical linearity errors are: 0.01% at 10kHz, 0.2% at 100kHz, 0.1% at 1MHz.
7. Exclusive of external components' drift.
8. FSR = Full Scale Range (corresponds to full scale and full scale input voltage.
9. Positive drift is defined to be increasing frequency with increasing temperature.
10. One pulse of new frequency plus 50nsec typical.

ABSOLUTE MAXIMUM RATINGS

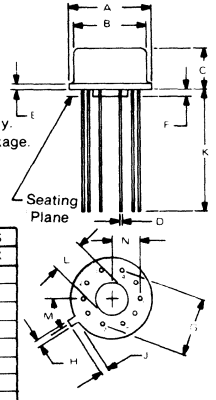
Supply Voltages	±20V
Output Sink Current at f_{OUT}	50mA
Output Current at V_{OUT}	+20mA
Input Voltage, -Input	$\pm V_{CC}$
Input Voltage, +Input	$\pm V_{CC}$
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10 seconds)	+300°C

MECHANICAL

VFC320BM/CM/SM TO-100 PACKAGE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

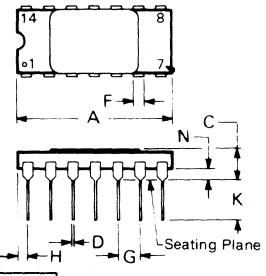


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
	.335	.370	8.51	9.40
	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.230 BASIC		5.84 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.70	
L	.120	.160	3.05	4.06
M	36° BASIC		36° BASIC	
N	.110	.120	2.79	3.05

VFC320BG/CG CERAMIC DUAL-IN-LINE

NOTE:
Leads in true position within 0.10" (0.25mm) R at MMC at seating plane.

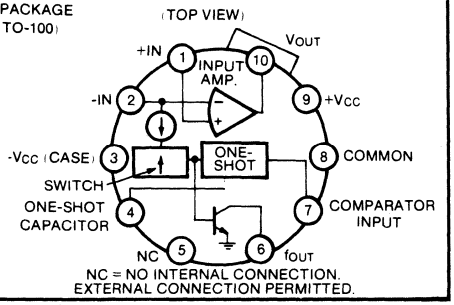
Pin numbers shown for reference only. Numbers may not be marked on package



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.670	.710	17.02	18.03
C	.065	.170	1.65	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.14	1.52
G	.100 BASIC		2.54 BASIC	
H	.025	.070	0.64	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.300 BASIC		7.62 BASIC	
M		10°		10°
N	.009	.060	0.23	1.52

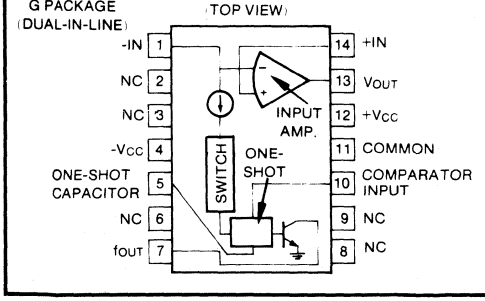
PIN CONFIGURATIONS

M PACKAGE (TO-100) (TOP VIEW)



NC = NO INTERNAL CONNECTION. EXTERNAL CONNECTION PERMITTED.

G PACKAGE (DUAL-IN-LINE) (TOP VIEW)



DISCUSSION OF SPECIFICATIONS

LINEARITY

Linearity is the maximum deviation of the actual transfer function from a straight line drawn between the end points (100% full scale input or frequency and 0.1% of full scale called zero). Linearity is the most demanding measure of voltage-to-frequency converter performance, and is a function of the full scale frequency. Refer to Figure 1 to determine typical linearity error for your application. Once the full scale frequency is chosen, the linearity is a function of operating frequency as it varies between zero and full scale. Examples for 10kHz full scale are shown in Figure 2. Best linearity is achieved at lower gains ($\Delta f_{OUT}/\Delta V_{IN}$) with operation as close to the chosen full scale frequency as possible.

The high linearity of the VFC320 makes the device an excellent choice for use as the front end of A/D converters with 12- to 14-bit resolution, and for highly accurate transfer of analog data over long lines in noisy environments (2-wire digital transmission).

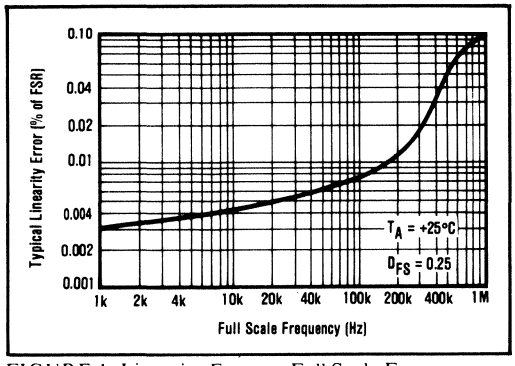


FIGURE 1. Linearity Error vs Full Scale Frequency.

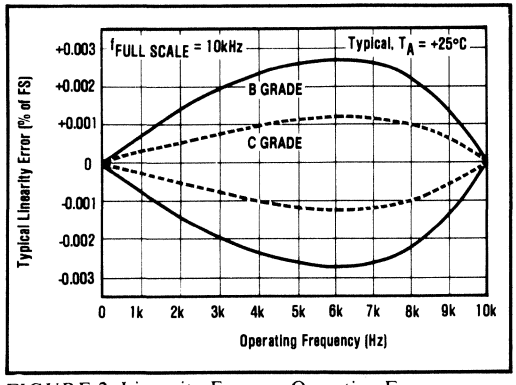


FIGURE 2. Linearity Error vs Operating Frequency.

FREQUENCY STABILITY VS TEMPERATURE

The full scale frequency drift of the VFC320 versus temperature is expressed as parts per million of full scale range per °C. As shown in Figure 3, the drift increases above 10kHz. To determine the total accuracy drift over temperature, the drift coefficients of external components (especially R_1 and C_1) must be added to the drift of the VFC320.

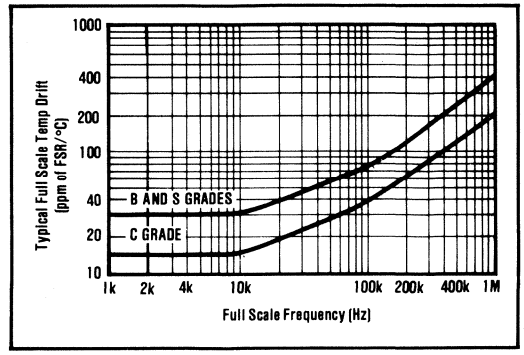


FIGURE 3. Full Scale Drift vs Full Scale Frequency.

RESPONSE

Response of the VFC320 to changes in input signal level is specified for a full scale step, and is 50nsec plus 1 pulse of the new frequency. For a 10V input signal step with the VFC320 operating at 100kHz full scale, the settling time to within ±0.01% of full scale is 10μsec.

THEORY OF OPERATION

The VFC320 monolithic voltage-to-frequency converter provides a digital pulse train output whose repetition rate is directly proportional to the analog input voltage. The circuit shown in Figure 4 is composed of an input amplifier, two comparators and a flip-flop (forming a one-shot), two switched current sinks, and an open collector output transistor stage. Essentially the input amplifier acts as an integrator that produces a two-part ramp. The first part is a function of the input voltage, and the second part is dependent on the input voltage and current sink. When a positive input voltage is applied at V_{IN}, a current will flow through the input resistor, causing the voltage at V_{OUT} to ramp down toward zero, according to $dV/dt = V_{IN}/R_1C_1$. During this time the constant current sink is disabled by the switch. Note, this period is only dependent on V_{IN} and the integrating components.

When the ramp reaches a voltage close to zero, comparator A sets the flip-flop. This closes the current sink switches as well as changing f_{OUT} from logic 0 to logic 1. The ramp now begins to ramp up, and 1mA charges through C_1 until V_{C1} = -7.5V. Note this ramp period is dependent on the 1mA current sink, connected to the negative input of the op amp, as well as the input voltage. At this -7.5V threshold point at C_1, comparator B resets the flip-flop, and the ramp voltage begins to ramp down again before the input amplifier has a chance to saturate. In effect the comparators and flip-flop form a one-shot whose period is determined by the internal reference and a 1mA current sink plus the external capacitor, C_1. After the one-shot resets, f_{OUT} changes back to logic 0 and the cycle begins again.

The transfer function for the VFC320 is derived for the

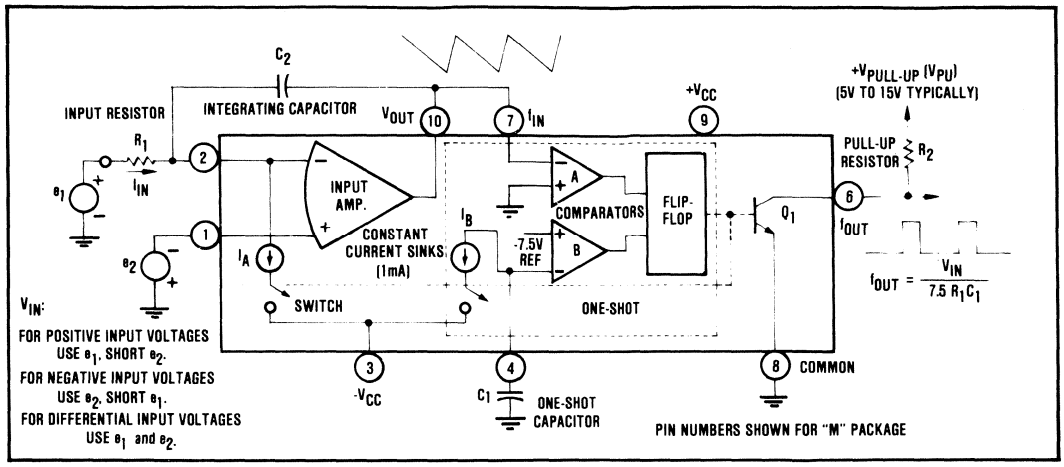


FIGURE 4. Functional Block Diagram of the VFC320.

the circuit shown in Figure 4. Detailed waveforms are shown in Figure 5.

$$f_{OUT} = \frac{1}{t_1 + t_2} \quad (1)$$

In the time $t_2 + t_1$ the integrator capacitor C_2 charges and discharges but the net voltage change is zero.

$$\text{Thus } \Delta Q = 0 = I_{IN}\, t_1 + (I_{IN} - I_A)\, t_2 \quad (2)$$

$$\text{So that } I_{IN}\,(t_1 + t_2) = I_A\, t_2 \quad (3)$$

$$\text{But since } t_1 + t_2 = \frac{1}{f_{OUT}} \text{ and } I_{IN} = \frac{V_{IN}}{R_1} \quad (4), (5)$$

$$f_{OUT} = \frac{V_{IN}}{I_A R_1 t_2} \quad (6)$$

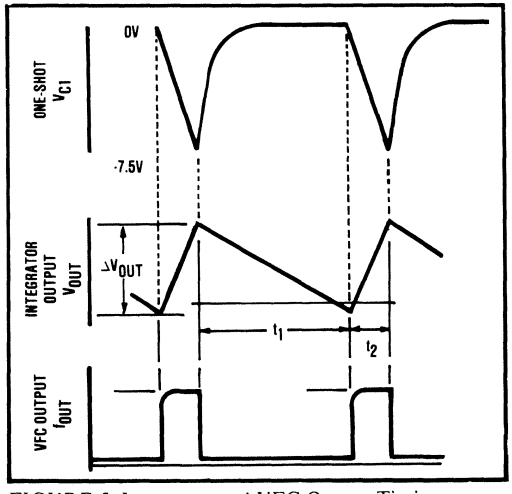


FIGURE 5. Integrator and VFC Output Timing.

In the time t_2, I_B charges the one-shot capacitor C_1 until its voltage reaches -7.5V and trips comparator B.

$$\text{Thus } t_2 = \frac{C_1\, 7.5}{I_B} \quad (7)$$

$$\text{Using (7) in (6) yield } f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \times \frac{I_B}{I_A} \quad (8)$$

$$\text{Since } I_A = I_B \text{ the result is}$$

$$f_{OUT} = \frac{V_{IN}}{7.5\, R_1 C_1} \quad (9)$$

Since the integrating capacitor, C_2, affects both the rising and falling segments of the ramp voltage, its tolerance and temperature coefficient do not affect the output frequency. It should, however, have a leakage current that is small compared to I_{IN}, since this parameter will add directly to the gain error of the VFC. C_1, which controls the one-shot period, should be very precise since its tolerance and temperature coefficient add directly to the errors in the transfer function.

The operation of the VFC320 as a highly linear frequency-to-voltage converter, follows the same theory of operation as the voltage-to-frequency converter. e_1 and e_2 are shorted and F_{IN} is disconnected from V_{OUT}. F_{IN} is then driven with a signal which is sufficient to trigger comparator A. The one-shot period will then be determined by C_1 as before, but the cycle repetition frequency will be dictated by the digital input at F_{IN}.

DUTY CYCLE

The duty cycle (D) of the VFC is the ratio of the one-shot period (t_2) or pulse width, PW, to the total VFC period ($t_1 + t_2$). For the VFC320, t_2 is fixed and $t_1 + t_2$ varies as the input voltage. Thus the duty cycle, D, is a function of the input voltage. Of particular interest is the duty cycle at full scale frequency, D_{FS}, which occurs at full scale input. D_{FS} is a user determined parameter which affects linearity.

$$D_{FS} = \frac{t_2}{t_1 + t_2} = PW \times f_{FS}$$

Best linearity is achieved when D_{FS} is 25%. By reducing equations (7) and (9) it can be shown that

$$D_{FS} = \frac{V_{IN}\ max\ /\ R_1}{1mA} = \frac{I_{IN}\ max}{1mA}$$

Thus $D_{FS} = 0.25$ corresponds to I_{IN} max = 0.25mA.

INSTALLATION AND OPERATING INSTRUCTIONS

VOLTAGE-TO-FREQUENCY CONVERSION

The VFC62 can be connected to operate as a V/F converter that will accept either positive or negative input voltages, or an input current. Refer to Figures 6 and 7.

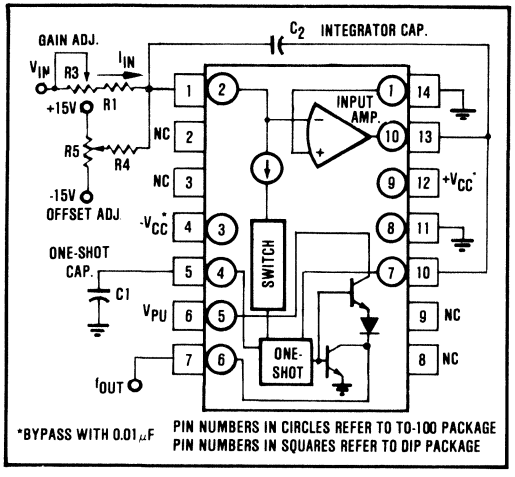


FIGURE 6. Connection Diagram for V/F Conversion, Positive Input Voltages.

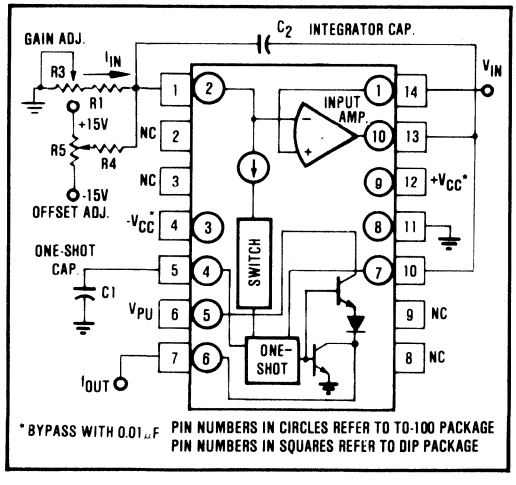


FIGURE 7. Connection Diagram for V/F Conversion, Negative Input Voltages.

EXTERNAL COMPONENT SELECTION

In general the design sequence consists of: (1) choosing f_{MAX}, (2) choosing the duty cycle at full scale ($D_{FS} = 0.25$ typically), (3) determining the input resistor, R_1 (Figure 4), (4) calculating the one-shot capacitor, C_1, and (5) selecting the integrator capacitor C_2.

Input Resistors R_1 and R_3

The input resistance (R_1 and R_3 in Figures 6 and 7) is calculated to set the desired input current at full scale input voltage. This is normally 0.25mA to provide a 25% duty cycle at full scale input and output. Values other than $D_{FS} = 0.25$ may be used but linearity will be affected. The nominal value of R_1 is

$$R_1 = \frac{V_{IN}\ max}{0.25mA} \qquad (10)$$

If gain trimming is to be done, the nominal value is reduced by the tolerance of C_1 and the desired trim range. R_1 should have a very-low temperature coefficient since its drift adds directly to the errors in the transfer function.

One-Shot Capacitor, C_1

This capacitor determines the duration of the one-shot pulse. From equation (9) the nominal value is

$$C_{1\ nom} = \frac{V_{IN}}{7.5\ R_1\ f_{OUT}} \qquad (11)$$

For the usual 25% duty at $f_{MAX} = V_{IN}/R_1 = 0.25mA$ there is approximately 15pF of residual capacitance so that the design value is

$$C_1\ (pF) = \frac{33 \times 10^6}{f_{FS}} - 15 \qquad (12)$$

where f_{FS} is the full scale output frequency in Hz. The temperature drift of C_1 is critical since it will add directly to the errors of the transfer function. An NPO ceramic type is recommended. Every effort should be made to minimize stray capacitance associated with C_1. It should be mounted as close to the VFC62 as possible. Figure 8 shows pulse width and full scale frequency for various values of C_1 at $D_{FS} = 25\%$.

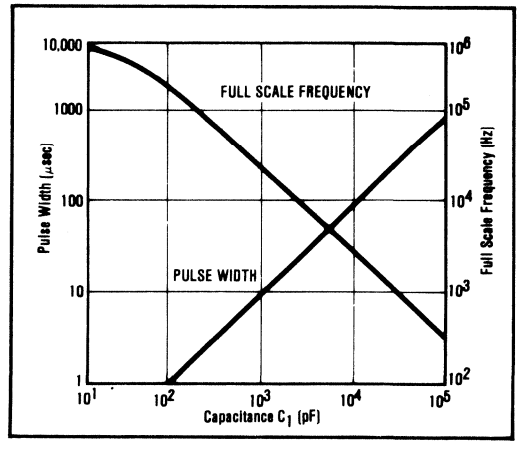


FIGURE 8. Output Pulse Width ($D_{FS} = 0.25$) and Full Scale Frequency vs External One-shot Capacitance.

Integrating Capacitor, C_2

Since C_2 does not occur in the V/F transfer function equation (9), its tolerance and temperature stability are not important; however, leakage current in C_2 causes a gain error. A ceramic type is sufficient for most applications. The value of C_2 determines the amplitude of V_{OUT}. Input amplifier saturation, noise levels for the comparators and slew rate limiting of the integrator

determine a range of acceptable values,

$$C_2\,(\mu F) = \begin{cases} \frac{100}{f_{FS}}\ ;\ \text{if } f_{FS} \leq 100kHz \\ 0.001;\ \text{if } 100kHz < f_{FS} \leq 500kHz \\ 0.0005;\ \text{if } f_{FS} > 500kHz \end{cases} \qquad (13)$$

Trimming Components R_3, R_4, R_5

R_5 nulls the offset voltage of the input amplifier. It should have a series resistance between 10kΩ and 100kΩ and a temperature coefficient less than 100ppm/°C. R_4 can be a 10% carbon film resistor with a value of 10MΩ.

R_3 nulls the gain errors of the converter and compensates for intitial tolerances of R_1 and C_1. Its total resistance should be at least 20% of R_1, if R_1 is selected 10% low. Its temperature coefficient should be no greater than five times that of R_1, to maintain a low drift of the R_3 - R_1 series combination.

OFFSET AND GAIN ADJUSTMENT PROCEDURES

To null errors to zero, follow this procedure:

1. Apply an input voltage that should produce an output frequency of 0.001 x full scale.
2. Adjust R_5 for proper output.
3. Apply the full scale input voltage.
4. Adjust R_3 for proper output.
5. Repeat steps 1 through 4.

If nulling is unnecessary for the application, delete R_4 and R_5, and replace R_3 with a short circuit.

POWER SUPPLY CONSIDERATIONS

The power supply rejection ratio of the VFC62 is 0.015% of FSR/% maximum. To maintain ±0.015% conversion, power supplies which are stable to within ±1% are recommended. These supplies should be bypassed as close as possible to the converter with 0.01μF capacitors.

DESIGN EXAMPLE

Given a full scale input of +10V, select the values of R_1, R_2, R_3, C_1, and C_2 for a 25% duty cycle at 100kHz maximum operation into one TTL load. See Figure 6.

Selecting C_1 ($D_{FS} = 0.25$)

$C_1 = [(33 \times 10^6)/f_{MAX}] - 15$ $\quad [(66 \times 10^6)/f_{MAX}] - 15$ if $D_{FS} = 0.5$

$= [(33 \times 10^6)/100kHz] - 15$

$= 315pF$

Choose a 300pF NPO ceramic capacitor with 1% to 10% tolerance.

Selecting R_1 and R_3 ($D_{FS} = 0.25$)

$R_1 + R_3 = V_{IN}\ max/0.25mA$ $\quad V_{IN}\ max/0.5mA$ if $D_{FS} = 0.5$

$= 10V/0.25mA$

$= 40k\Omega$

Choose 32.4kΩ metal film resistor with 1% tolerance and R_3 = 10kΩ cermet potentiometer.

Selecting C_2

$C_2 = 10^2/F_{max}$

$= 10^2/100kHz$

$= 0.001\mu F$

Choose a 0.001μF capacitor with ±5% tolerance.

FREQUENCY-TO-VOLTAGE CONVERSION

To operate the VFC62 as a frequency-to-voltage converter, connect the unit as shown in Figure 9. To interface with TTL-logic, the input should be coupled through a capacitor, and the input to pin 10 biased near +2.5V. The converter will detect the falling edges of the input pulse train as the voltage at pin 10 crosses zero. Choose C_3 to make t = 0.1T (see Figure 9). For input signals with amplitudes less than 5V, pin 10 should be biased closer to zero to insure that the input signal at pin 10 crosses the zero threshold. Errors are nulled following the procedure given on this page, using 0.001 x full scale frequency to null offset, and full scale frequency to null the gain error. Use equations from V/F calculations to find R_1, R_3, R_4, R_5, C_1 and C_2.

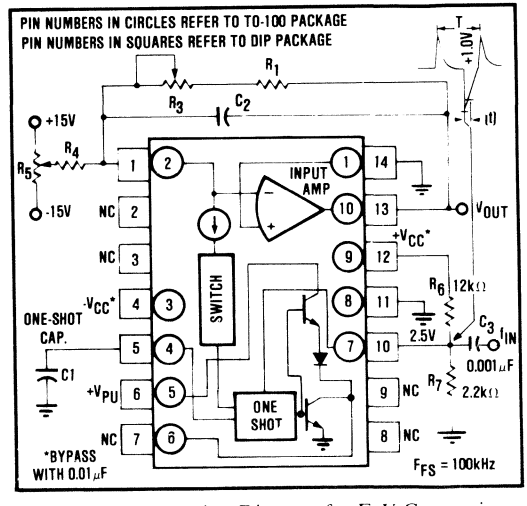


FIGURE 9. Connection Diagram for F V Conversion.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC62 ideal for a variety of VFC applications. High accuracy allows the VFC62 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC62.

TYPICAL APPLICATIONS

Excellent linearity, wide dynamic range, and compatible TTL, DTL, and CMOS digital output make the VFC320 ideal for a variety of VFC applications. High accuracy allows the VFC320 to be used where absolute or exact readings must be made. It is also suitable for systems requiring high resolution up to 14 bits.

Figures 10 - 14 show typical applications of the VFC320.

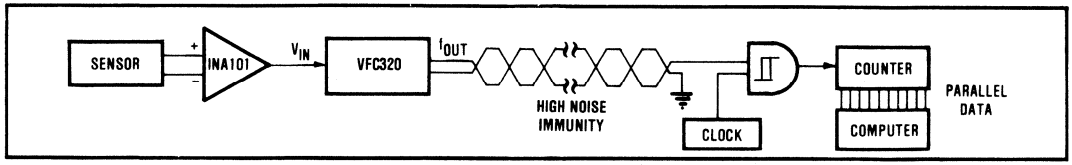


FIGURE 10. Inexpensive A/D with Two-Wire Digital Transmission Over Twisted Pair.

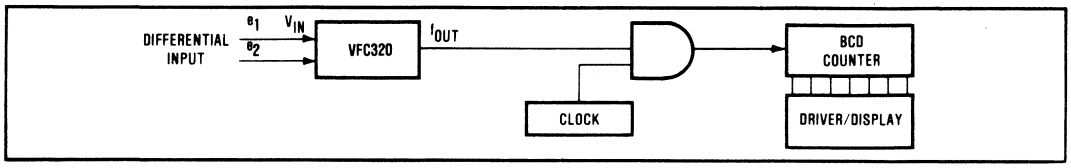


FIGURE 11. Inexpensive Digital Panel Meter.

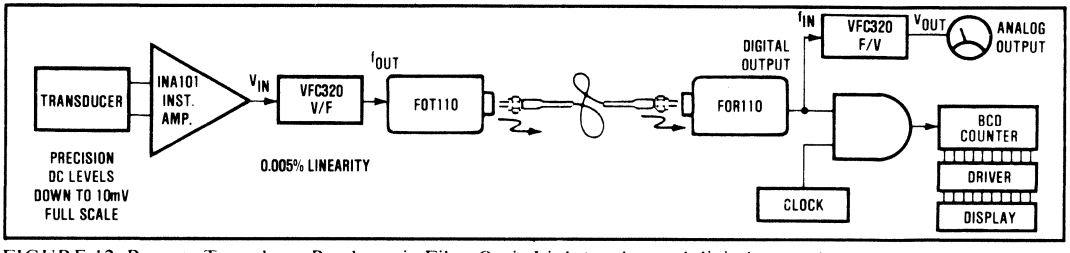


FIGURE 12. Remote Transducer Readout via Fiber Optic Link (analog and digital output).

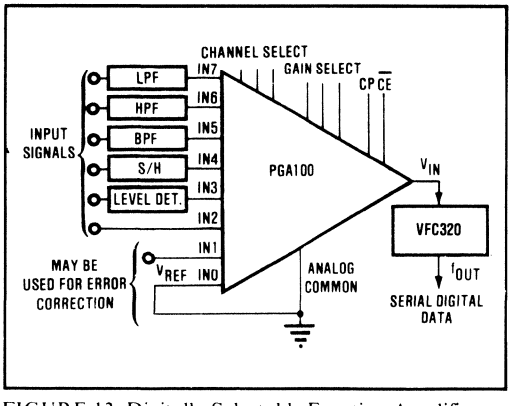


FIGURE 13. Digitally Selectable Function Amplifier with Serial Data Output.

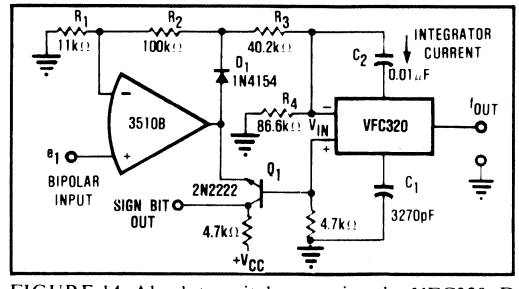
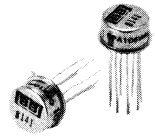


FIGURE 14. Absolute switchover using the VFC320. D_1 and Q_1 switch on alternately as polarity of input signal changes, thus maintaining direction of integrator current. V/F converter cannot distinguish between signal polarities of the same magnitude and so generate the same frequency for both.

BURR-BROWN®

OPA106/MIL SERIES



MODEL NUMBERS:

OPA106WM/MIL	OPA106VM/MIL
OPA106WM/883B	OPA106VM/883B
OPA106WM	OPA106VM
OPA106UM/883B	REVISION NONE
OPA106UM	JULY, 1982

FET Input Military OPERATIONAL AMPLIFIER

FEATURES

- LOW BIAS CURRENT, 100fA, max
- HIGH INPUT IMPEDANCE, $10^{13}\Omega$
- LOW DRIFT, $5\mu V/°C$, max
- LOW OFFSET VOLTAGE $250\mu V$, max
- LOW QUIESCENT CURRENT, 1.5mA, max
- HERMETICALLY SEALED TO-99 PACKAGE

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS

DESCRIPTION

The OPA106/MIL Series is a low bias current 100fA, max) operational amplifier. Guaranteed low initial offset voltage ($250\mu V$, max) and associated drift versus temperature ($5\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. This feature, and guaranteed low bias current allow greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA106/MIL Series include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA106/MIL Series allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.

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DETAILED SPECIFICATION
MICROCIRCUITS, LINEAR
OPERATIONAL AMPLIFIER
HYBRID, SILICON

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a FET input, low bias current, low drift, integrated circuit operational amplifier.

1.2 Part Number. The complete part number is as shown below.

OPA106	V	M	/MIL
Basic model number	Grade (see 1.2.1)	Metal package	Hi-Rel product designator (see 1.2.2)

1.2.1 Device type. The device is a single operational amplifier. Three electrical performance grades are provided. The W grade features $\pm 5\mu V/^{\circ}C$ drift (-55°C to +125°C). The V grade features $\pm 10\mu V/^{\circ}C$ drift (-55°C to +125°C). The U grade features $\pm 20\mu V/^{\circ}C$ drift from -25°C to +85°C and guarantees performance from -55°C to +125°C.

Electrical specifications are shown in Table I. Electrical tests are shown in Tables II and III.

1.2.2 Device class. The device class is similar to the hybrid class (class B) product assurance level, as defined in MIL-M-38510. The Hi-Rel product designator portion of the part number distinguishes the product assurance levels as follows:

Hi-Rel product designator	Requirements
/MIL	Standard model, plus 100% MIL-STD-883 hybrid class screening, with 10% PDA, plus quality conformance inspection (QCI) consisting of Groups A and B on each inspection lot, plus Groups C and D performed initially and periodically thereafter. Additional electrical testing is performed on /MIL models.
883B	Standard model, plus 100% MIL-STD-883 hybrid class screening.
(none)	Standard model including 100% electrical testing.

1.2.3 Case outline. The case outline is A-1 (8-lead can, TO-99) as defined in MIL-M-38510, Appendix C. The case is metal and is conductive.

1.2.4 Absolute maximum ratings.

Supply voltage range	±20VDC
Input voltage range	±20VDC [1]
Differential input voltage range	±40VDC [1]
Storage temperature range	-65°C to +150°C
Output short-circuit duration	Unlimited [2]
Lead temperature (soldering, 60sec)	300°C
Junction temperature	T_J = +175°C

1.2.5 Recommended operating conditions.

Supply voltage range	±5VDC to ±20VDC
Ambient temperature range	-55°C to +125°C

1.2.6 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ J-C
8-lead can	Figure 1	225mW at T_A = +125°C	220°C/W

1 The absolute maximum input voltage is equal to the supply voltage.
2 Short circuit may be to ground only. Rating applies to +135°C case temperature or +50°C ambient temperature at ±15VDC supply voltage.

2. APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, general specification for.

STANDARD

MILITARY

MIL-STD-883 - Test methods and procedures for microcircuits.

3. REQUIREMENTS

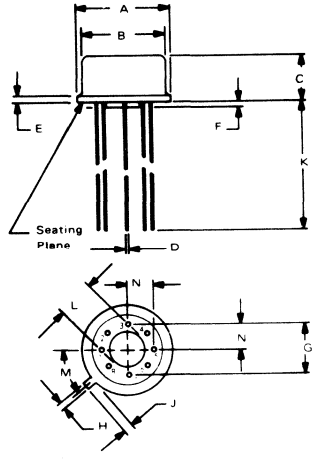
3.1 General. Burr-Brown uses production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with this specification.

3.1.1 Detail specifications. The individual item requirements are specified herein. In the event of conflicting requirements the order of precedence will be the purchase order, this specification, and then the reference documents.

3.1.2 Country of manufacture. These microcircuits are manufactured, assembled, and tested within the United States of America.

3.2 Design, construction, and physical dimensions.

3.2.1 Package, metals, and other materials. The package is in accordance with paragraph 3.5.1 of MIL-M-38510. The exterior metal surfaces are corrosion resistant. The other materials are nonnutrient to fungus as specified in MIL-M-38510. See Figure 1 for the case outline.



Note:
Leads in true position within 0.010" 0.25mm R at MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

FIGURE 1. Case Outline (TO-99) Package Configuration.

3.2.2 Design documentation. The design documentation is in accordance with MIL-M-38510.

3.2.3 Internal conductors and internal lead wires. The internal conductors and internal lead wires are in accordance with MIL-M-38510.

3.2.4 Lead material and finish. The lead material is kovar type (type A). The lead finish is gold plate with nickel underplating. The lead material and finish is in accordance with MIL-M-38510 and is solderable per MIL-STD-883, method 2003.

3.2.5 Die thickness. The die thickness is in accordance with MIL-M-38510.

3.2.6 Physical dimensions. The physical dimensions are in accordance with paragraph 1.2.3 herein.

3.2.7 Circuit diagram and terminal connections. The circuit diagram and terminal connections are shown in Figure 2.

3.2.8 Glassivation. All dice utilized are glassivated.

3.2.9 Schematic Circuit. The schematic circuit is shown in Figure 3.

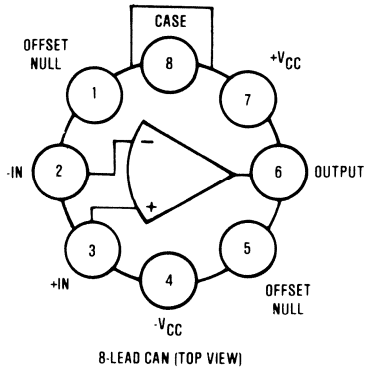


FIGURE 2. Circuit Diagram and Terminal Connections.

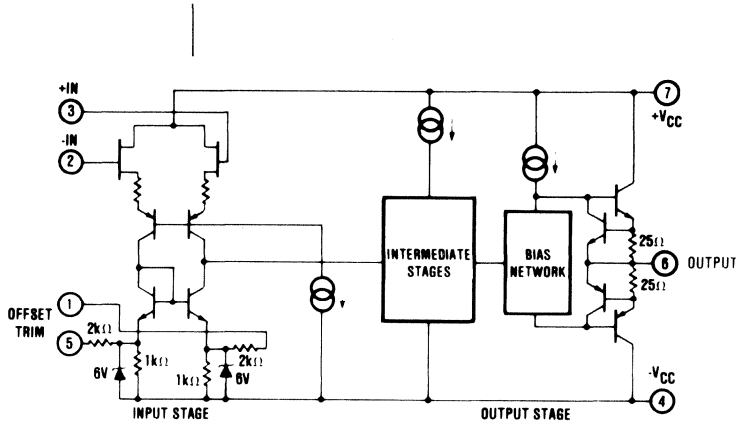


FIGURE 3. Simplified Schematic Circuit.

3.3 Electrical performance characteristics. The electrical performance characteristics are as specified in Table I and apply over the full operating ambient temperature range of -55°C to +125°C unless otherwise specified.

3.3.1 Additional electrical performance characteristics. Electrical performance curves are shown in paragraph 7.

3.3.2 Offset null. The amplifier is capable of being nulled to zero offset voltage using the circuit in Figure 4. If nulling is unnecessary for the application, delete the potentiometer and make no connections.

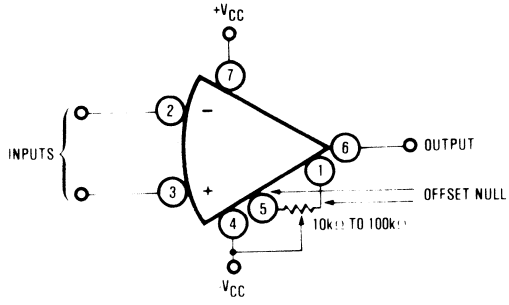


FIGURE 4. Offset Null Circuit.

3.3.3 Frequency compensation. No frequency compensation is required. The amplifier is free of oscillation when operated at any gain and when operated in any test condition specified herein.

3.4 Electrical tests. Electrical tests are shown in Table II. The subgroups of Table III and limits of Table IV, which constitute the minimum electrical tests for screening, qualification, and quality conformance, are shown in Table II.

3.5 Marking. Marking is in accordance with MIL-M-38510. The following marking is placed on each microcircuit as a minimum.

a. Part number (see paragraph 1.2)
b. Inspection lot identification code 1/
d. Manufacturer's identification (BURR-BROWN®)
e. Manufacturer's designating symbol (CEBS)
f. Country of origin (U.S.A)

3.6 Workmanship. These microcircuits are manufactured, processed, and tested in a careful and workmanlike manner. Workmanship is in accordance with good engineering practices, workmanship instructions, inspection and test procedures, and training, prepared in fulfillment of Burr-Brown's product assurance program.

3.6.1 Rework provisions. Rework provisions, including rebonding for the MIL product designation, are in accordance with MIL-M-38510.

3.7 Traceability. Traceability for MIL product designation is in accordance with MIL-M-38510. Each microcircuit is traceable to the production lot and to the component vendor's component lot. Reworked or repaired microcircuits maintain traceability.

3.8 Product and process change. Burr-Brown will not implement any major change to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality or interchangeability of the microcircuit without full or partial requalification.

1/ A 4-digit date code, indicating year and week of seal, is marked on 883B and (none) Hi-Rel product designations.

TABLE I. Electrical Performance Characteristics.

All characteristics at -55°C ≤ T_A ≤ +125°C, ±V_{CC} = 15VDC, unless otherwise specified.

CHARACTERISTIC	SYMBOL	CONDITIONS	OPA106WM/MIL** OPA106WM/883B OPA106WM			OPA106VM/MIL** OPA106VM/883B OPA106VM			OPA106UM/883B OPA106UM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN												
Open-Loop Voltage Gain	A_{VS}	R_L = 2kΩ, V_O = ±10V, F = 0Hz; T_A = +25°C	103	109		•	•		•	•		dB
		-55°C ≤ T_A ≤ +125°C	93	101		•	•		•	•		dB
RATED OUTPUT												
Voltage	V_O	R_L = 1kΩ	±10			•			•			V
Current	I_O		±10			•			•			mA
Impedance	Z_O	T_A = +25°C		3			•			•		kΩ
Load Capacitance	C_L	T_A = +25°C	500	1000		•	•		•	•		pF
Short Circuit Current	I_{OS}	To Ground	10	25		•	•		•	•		mA
DYNAMIC RESPONSE												
Bandwidth	BW	Unity Gain-Small, Signal T_A = +25°C		1			•			•		MHz
Bandwidth	BW	Full Power T_A = +25°C	19	28		•	•		•	•		kHz
Slew Rate	SR	R_L = 2kΩ, T_A = +25°C	1.2	1.8		•	•		•	•		V/μsec
Settling Time (0.1%)	T_S	T_A = +25°C		6			•			•		μsec
Settling Time (0.01%)	T_S	T_A = +25°C		18			•			•		μsec
Overload Recovery 1/	T_r	T_A = +25°C		4	15		•	•		•	•	μsec
INPUT OFFSET VOLTAGE												
Initial Offset	V_{IO}	T_A = +25°C			±250			•			•	μV
Temperature Sensitivity	DV_{IO}	$\frac{V_{IO}(T_A) - V_{IO}(+25°C)}{\Delta T}$										
		-55°C ≤ T_A ≤ +125°C			±5			±10			50	μV/°C
		-25°C ≤ T_A ≤ +85°C									±20	μV/°C
vs Power Supply	PSRR	V_{CC} = ±5, V_{CC} = ±20VDC			±80			•			•	dB
INPUT BIAS CURRENT												
Initial Bias	I_{ib}	T_A = +25°C			100			-150			-300	fA
vs Supply Voltage		T_A = +25°C		1			•			•		fA/V
INPUT OFFSET CURRENT 2/												
Initial Offset	I_{IO}	T_A = +25°C		±40			±80			±80		fA
INPUT IMPEDANCE												
Differential	Z_{ID}	T_A = +°C		10^{13} || 0.8			•			•		Ω || pF
Common-Mode	Z_{ICM}			10^{15} || 1.6			•			•		Ω || pF
INPUT NOISE												
Voltage	e_n	f_O = 10Hz T_A = +25°C		75			•			•		$nV/\sqrt{Hz}$
		f_O = 100Hz T_A = +25°C		55			•			•		$nV/\sqrt{Hz}$
		f_O = 1kHz T_A = +25°C		35			•			•		$nV/\sqrt{Hz}$
		f_O = 10kHz T_A = +25°C		35			•			•		$nV/\sqrt{Hz}$
		f_B = 0.1Hz to 10Hz T_A = +25°C		6			•			•		μV/, p-p
Current	i_n	f_B = 0.1Hz to 10Hz T_A = +25°C		3			•			•		fA, p-p
		f_B = 10Hz to 10kHz T_A = +25°C		10			•			•		fA, rms
		f_O = 1kHz T_A = +25°C		0.25			•			•		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE												
Differential	V_{di}	T_A = +25°C	±20			•			•			V
Common-Mode		T_A = +25°C	±10	±12		•	•		•	•		V
Common-Mode Rejection	CMRR	V_{IN} = ±10V T_A = +25°C	76	86		•	•		•	•		dB
POWER SUPPLY												
Rated Voltage	±V_{CC}			±15			•			•		VDC
Voltage Range			±5		±20	•		•	•		•	VDC
Quiescent Current	I_Q			1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)												
Operating			-55		+125	•		•	•		•	°C
Storage			-65		+150	•		•	•		•	°C

*Same as OPA106W Grade **OPA106WM/MIL and OPA106VM/MIL available 2nd quarter 1983.

NOTES:

1/ Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.

2/ Bias current is tested and guaranteed at T_A = +25°C. For higher temperature the bias current doubles every +10°C.

3.9 Screening. Screening, for /MIL and /883B Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, except as modified in paragraph 4.3 herein.

Screening for the standard model includes Burr-Brown QC4118 internal visual inspection and stabilization bake, fine leak, gross leak, burn-in (72 hours performed preseal), temperature cycle (condition C), constant acceleration (condition B), and external visual inspection per MIL-STD-883, method 5008, hybrid class.

For the /MIL product designation, all microcircuits will have passed the screening requirements prior to qualification or quality conformance inspection.

3.10 Qualification. Qualification is not required. See paragraph 4.2 herein.

3.11 Quality conformance inspection. Quality conformance inspection, for /MIL product designation, is in accordance with MIL-M-38510, except as modified in paragraph 4.4 herein. The microcircuit inspection lot will have passed quality conformance inspection prior to microcircuit delivery.

TABLE II. Electrical Test Requirements.

(The individual tests within the subgroups appear in Table III)

MIL-STD-883B REQUIREMENTS (hybrid class) / MODELS	OPA106WM/MIL	OPA106WM/883B OPA106WM	OPA106VM/MIL	OPA106VM/883B OPA106VM	OPA106UM/883B OPA106UM
Interim electrical parameters (pre burn-in) (method 5008)	1, 4	1, 4	1, 4	1, 4	1, 4
Final electrical test parameters (method 5008)	1*, 2, 3, 4	1, 2, 3, 4	1*, 2, 3, 4	1, 2, 3, 4	1, 2U, 3U, 4
Group A test requirements (method 5008)	1, 2, 3, 4	---	1, 2, 3, 4	---	---
Group C end point electrical parameters (method 5008)	Table IV limits and delta limits	---	Table IV limits and delta Limits	---	---
Additional electrical subgroups for Group C inspections	5, 6 1/	---	5, 6 1/	---	---

*PDA applies to subgroups 1 - 4 (see 4.3.d)

1/LTPD 15%

TABLE III. Group A Inspection.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD OR EQUIVALENT	CONDITIONS $\pm V_{CC}$ = 15VDC unless otherwise specified	LIMITS						UNITS
				OPA106WM/MIL OPA106WM/883B OPA106WM		OPA106VM/MIL OPA106VM/883B OPA106WM		OPA106UM/883B OPA106UM		
				MIN	MAX	MIN	MAX	MIN	MAX	
	V_{IO}	4001			±250		±250		±250	µV
	I_{IB}	4001			±100		±150		±300	fA
	V_O		R_L = 2kΩ	±10		±10		±10		V
1	I_Q				1.5		1.5		1.5	mA
T_A = +25°C	CMRR	4003	V_{CM} ±10V	76		76		76		dB
	PSRR		V_{CC} = ±5V, V_{CC} = ±20V	80		80		80		dB
2 T_A = +125°C	DV_{IO}	4001	$\frac{V_{IO}\ (125) - V_{IO}\ (25)}{100}$		5		10			µV/°C
2U T_A = +85°C	DV_{IO}	4001	$\frac{V_{IO}\ (85) - V_{IO}\ (25)}{60}$						20	µV/°C
3 T_A = -55°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-55)}{80}$		5		10			µV/°C
3U T_A = -25°C	DV_{IO}	4001	$\frac{V_{IO}\ (25) - V_{IO}\ (-25)}{50}$						20	µV/°C
4	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	103		103		103		dB
T_A = +25°C	SR	4002	R_L = 2kΩ V_O = ±10V	1.2		1.2		1.2		V/µsec
5 T_A = +125°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB
6 T_A = -55°C	A_{VS}	4004	f = 0Hz, R_L = 2kΩ	93		93				dB

TABLE IV. Group C, End Point Electrical Parameters.
(T_A = +25°C, ±V_{CC} = 15VDC, V_{DD} = +5VDC)

TEST	LIMIT	DELTA
V_{IO}	±250μV	±125μV

4. PRODUCT ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures are in accordance with MIL-M-38510 and MIL-STD-883, method 5008, except as modified herein.

4.2 Qualification. Qualification is not required unless specifically required by contract or purchase order. When so required, qualification will be in accordance with the inspection routine of MIL-M-38510, paragraph 4.4.2.1. The inspections to be performed are those specified herein for groups A, B, C and D inspections (see paragraphs 4.4.1, 4.4.2, 4.4.3, and 4.4.4).

Burr-Brown has performed and successfully completed qualification inspection as described above. The most recent report is available from Burr-Brown.

4.3 Screening. Screening, for /MIL and /883 Hi-Rel product designations, is in accordance with MIL-STD-883, method 5008, hybrid class, and is conducted on all devices. The following additional criteria apply:

a. Constant acceleration test (MIL-STD-883, method 2001) is test condition B, Y_1 axis only.

b. Interim and final test parameters are specified in Table II. The interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

B c. Burn-in test (MIL-STD-883, method 1015) conditions:

(1) Test condition B

(2) Test circuit is Figure 5 herein

(3) T_A = +125°C minimum

(4) Test duration is 160 hours minimum

d. Percent defective allowable (PDA). The PDA, for/MIL product designation only, is 10 percent and includes both parametric and catastrophic failures. It is based on failures from group A, subgroup 1 test, after cool-down as final electrical test in accordance with MIL-STD-883, method 5008, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from preburn-in screening failures may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in in that lot are used to determine the percent defective for that lot, and the lot is accepted or rejected based on the PDA.

e. External visual inspection need not include measurement of case and lead dimensions.

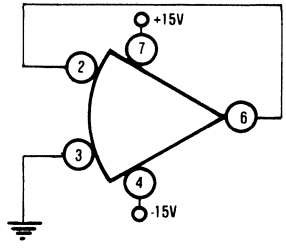


FIGURE 5. Test Circuit, Burn-in and Operating Life Test.

4.4 Quality conformance inspection. Groups A and B inspections of MIL-STD-883, method 5008, is performed on each lot. Groups C and D inspections of MIL-STD-883, method 5008, are not required unless specified by contract or purchase order.
specified by contract or purchase order.

Burr-Brown periodically performs groups C and D inspections of MIL-STD-883, method 5008. A report of the most recent groups C and D inspections is available from Burr-Brown.

4.4.1 Group A inspection. Group A inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table X, and as specified in Table II herein.

4.4.2 Group B inspection. Group B inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table XI.

4.4.3 Group C inspection. Group C inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table XII, and as follows:

a. Operating life test (MIL-STD-883, method 1005) conditions:
   (1) Test condition D
   (2) Test circuit is Figure 5 herein
   (3) $T_A = +125°C$ minimum.
   (4) Test duration is 1000 hours minimum
b. End point electrical parameters are specified in Table II herein.
c. Additional electrical subgroups are specified in Table II herein.

4.4.4 Group D inspection. Group D inspection consists of the test subgroups and LTPD values shown in MIL-STD-883, method 5008, Table V.

4.5 Methods of examination and test. Methods of examination and test are specified in the appropriate tables. Electrical test circuits are as prescribed herein or in the referenced test methods of MIL-STD-883.

4.5.1 Voltage and current. All voltage values given, except the input offset voltage (or differential voltage) are referenced to the external zero reference level of the supply voltage. Currents given are conventional current and positive when flowing into the referenced terminal.

4.6 Inspection of preparation for delivery. Inspection of preparation for delivery is in accordance with MIL-M-38510, except that the rough handling test does not apply.

5. PREPARATION FOR DELIVERY

5.1 Preservation-packaging and packing. Microcircuits are prepared for delivery in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for use in applications where the use of screened parts is desirable.

6.3 Ordering data. The contract or order should specify the following:

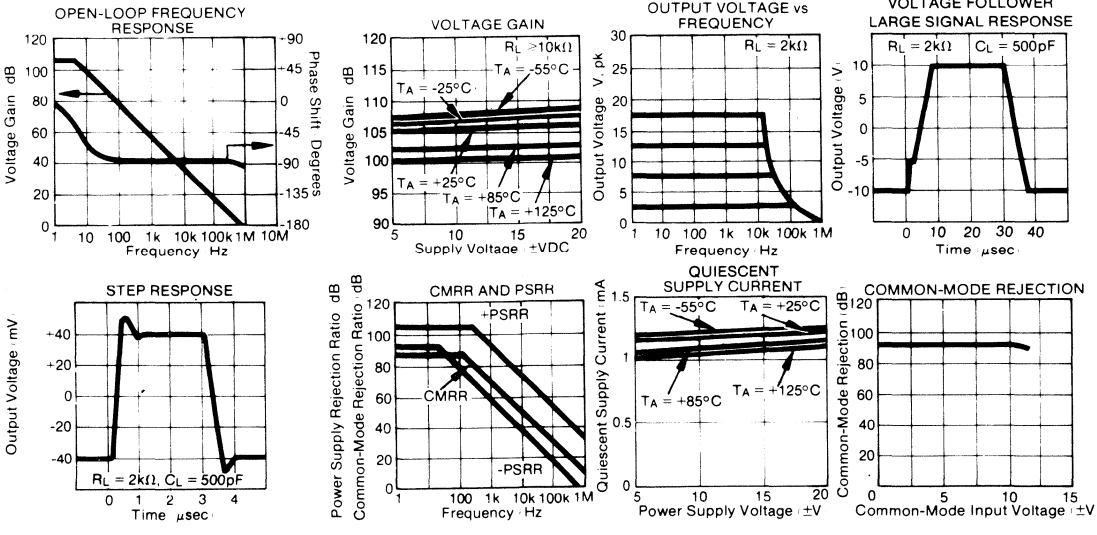
a. Complete part number (see paragraph 1.2)
b. Requirement for certificate of compliance, if desired.

6.4 Microcircuit group assignment. These microcircuits are assigned to Technology Group F as defined in MIL-M-38510, Appendix E.

6.5 Electrostatic sensitivity. These microcircuits may be damaged by electrostatic discharge. Electrostatic sensitive precautions should be observed at all times.

7. ELECTRICAL PERFORMANCE CURVES.

(Typical at $T_A = +25°C$ and $\pm V_{CC} = 15VDC$ unless otherwise specified).



8. APPLICATION INFORMATION

8.1 Offset voltage adjustment. Although the OPA106/MIL Series has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. Figure 4 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C for every 100μV of offset adjustment.

8.2 Guarding and shielding. The ultra-low bias current and high impedance of the OPA106/MIL Series are well-suited to a number of stringent applications, however, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA106/MIL Series.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA106/MIL Series. To avoid leakage problems, it is recommended that the signal input lead of the OPA106/MIL Series be wired to a Teflon standoff. If the OPA106/MIL Series is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low input impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 6 illustrates the use of the guard. The resistor R_3 shown in Figure 6 is optional. It may be used to compensate effects of very large source resistances. However, note that its use would also increase the noise due to the thermal noise of R_3.

8.3 Thermal response time. Thermal response time is an important parameter in low drift operational amplifiers like the OPA106/MIL Series. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA106/MIL Series is approximately 20 seconds.

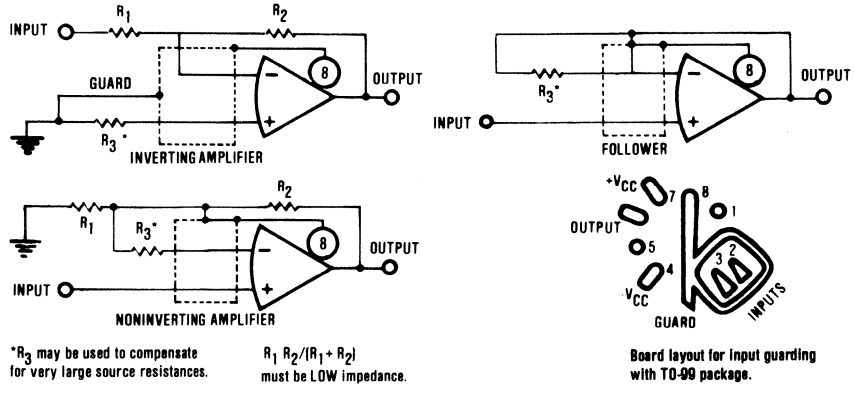


FIGURE 6. Connection of Input Guard.

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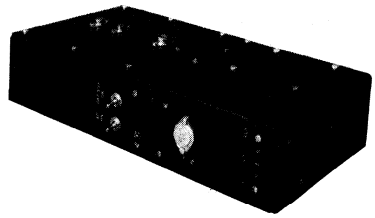

PSB100

ADVANCE INFORMATION
Subject to Change

REGULATED DC POWER SUPPLY WITH BATTERY BACK-UP

DESCRIPTION

Customers building critical control systems can now purchase a power supply with a self-contained battery back-up, eliminating the need for separate, expensive UPS systems.

PSB100 supplies all common voltages used in microcomputer systems, such as the Multibus™ system. The supply unit includes an internal 24V battery pack and charger, three TTL outputs and LED indicators that indicate power system status. Signals are provided for line power loss, low battery, and very low battery. Internal batteries provide a minimum of 30 minutes back-up at full load. An external 24VDC battery pack can be added to extend back-up time.

INPUT

Line Voltage	(1) 100-130VAC/200-260 VAC
Battery (Internal)	(2) 18-24 VAC 2.5AHR
Line Fuse	1.5ASB-115VAC/.75ASB-230VAC

(1) Operation above 130/260VAC may damage unit. 115/230VAC operation is switch selectable.

(2) An external 24VDC lead acid battery may be connected. No fuse protection is provided for the external battery.

OUTPUTS

		RIPPLE (MAX)	CURRENT	CURRENT LIMIT
+5VDC	±5%	150mV P-P	11.2A	12.0A ±5%
+12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-12VDC	±5%	360mV P-P	1.2A	1.5A ±5%
-5VDC	±1%	40mV	100mA	NONE

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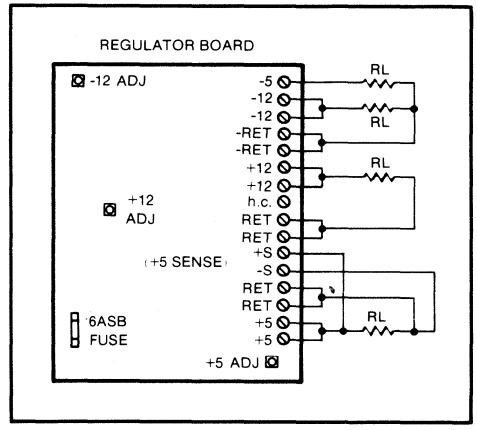

OPERATION

1. Insure proper line and load connection to unit.
2. Insure proper line voltage selection, 115/230VAC.
3. Place AC switch in ON position; the AC indicator should light. The unit is now operating.
4. Place BATTERY switch in ON position. Battery back-up of supply is now operational. Note that the supply is not battery-startable.
5. To turn unit off once started, both the AC switch and the BATTERY switch must be in the OFF position.

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BATTERY BACK-UP

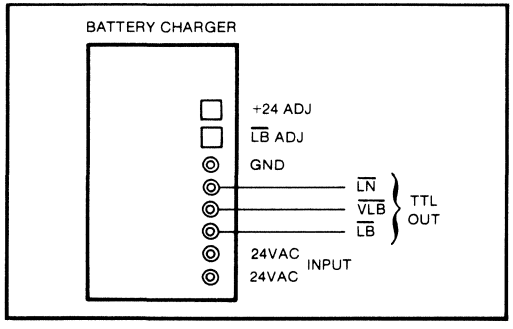
PSB100 contains a 24VDC 2.5 AHR lead acid battery pack. The battery is charged and maintained by an internal battery charger. Upon loss of AC power, the battery will maintain operation of a full load for 30 minutes minimum if fully charged. An external 24VDC rechargeable battery may be connected if desired. If an external battery is installed, the internal battery should be disconnected (remove battery fuse). The internal charger will supply 24VDC at 500mA to charge or maintain external batteries.

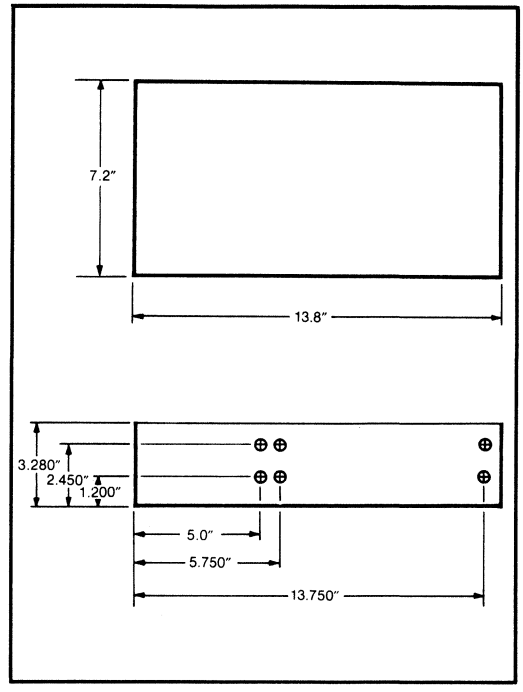
BATTERY CHARGER

24VDC at 500mA
Low battery (LB) indication 21VDC
Very low battery (VLB) indication 19.5VDC

LB and VLB indication are operational only during battery discharge cycle.

Three TTL compatible outputs are provided on the charger circuit board for low battery (LB), very low battery (VLB) and line loss (LN). All three outputs are active low.





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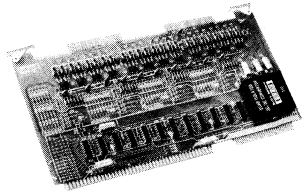
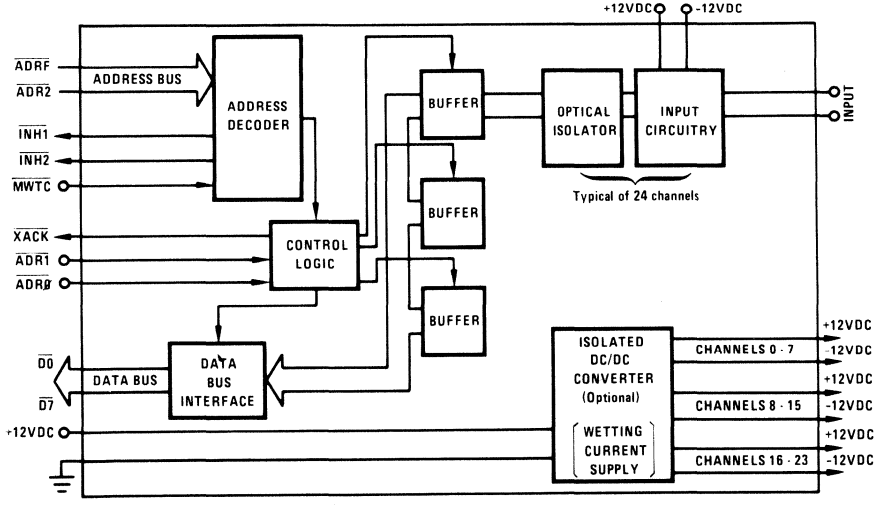


MP810
MP810-DB
MP810-NS
MP810-LV
MP810-AC

MICROCOMPUTER DIGITAL INPUT SYSTEM

A 24-CHANNEL ISOLATED DIGITAL INPUT SYSTEM COMPATIBLE WITH IEEE-796 (MULTIBUS™)



Multibus™ - Intel Corp.

FEATURES

- ISOLATION - FIELD TO COMPUTER
- ISOLATION - CHANNEL TO CHANNEL
- CONTACT CLOSURE
- CONTACT WETTING CURRENT
- VOLTAGE INPUTS DC/AC
- DEBOUNCE
- TTL-COMPATIBLE INPUTS
- 20-BIT ADDRESSABLE
- +70°C BURN-IN

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DESCRIPTION

The MP810 series provides 24 optically-isolated discrete inputs for Multibus (IEEE-796) based microcomputer systems. Input signal types include 1) dry contact closures, 2) wetted contact closures, 3) DC voltages, and 4) AC voltages. Isolation protects the computer from input voltage transients and malfunctions of field inputs. In addition, channel-to-channel isolation minimizes channel interaction and avoids ground loop problems.

Full hardware integration allows cards to be inserted directly into the system back panel. Power for the card is provided by the system bus; therefore, no external power supplies are required.

The MP810 is memory-mapped. Data is acquired through any memory read operation. Each input is 1 bit of an 8-bit word. An open contact (low voltage) is represented by a logic 0 and a closed contact (high voltage) is represented by logic 1.

Contact debounce is available on some models. This prevents erroneous data that could be caused by relay contact bounce. The hardware approach unburdens the processor and reduces system overhead normally required to debounce contact closures.

SPECIFICATIONS

Electrical

Typical at +25° C and rated supplies unless otherwise noted.

MODEL	MP810	MP810-DB	MP810-NS	MP810-LV	MP810-AC	UNITS
INPUT CHARACTERISTICS						
Number of Inputs	24	24	24	24	24	
Input Resistor	15K, 1/2W	15K, 1/2W	15K, 1/2W	1.5K, 1/2W	56K, 1/2W	Ω
Delay Times						
Open-to-Closed(1)	0.025	65(3)	0.025	0.025	1(3)	msec
Closed-to-Open(2)	0.100	65(3)	0.100	0.100	80(3)	msec
VOLTAGE SENSE						
Logic 0	Open(4)	Open(4)	4VDC	2VDC	10V rms(6)	V, max
Logic 1	Closed(4)	Closed(4)	17VDC	3.5VDC	48V rms(6)	V, min
MAXIMUM VOLTAGE (V_S) ACROSS INPUT WITHOUT DAMAGE						
VDC, max	60	60	84	20	120	VDC
VAC, max	120	120	168	40	250	VAC, rms
VOLTAGE SOURCE (contact wetting)	±12V	±12V	None	None	None	
ISOLATION VOLTAGE						
System-to-Field	600	600	600	600	600	VDC
Channel-to-Channel	(7)	(7)	300	300	300	VDC
Input Blocks(5)	600	600	600	600	600	VDC
POWER REQUIREMENTS	+5/+12	+5/+12	+5	+5	+5	VDC
	400/100	400/100	400	400	400	mA
BUS INTERFACE	Meets electrical and mechanical specifications of IEEE-796 (Multibus)					
ENVIRONMENT						
Operating Temperature	0 - +70° C					
Storage Temperature	-55° C to +125° C					
Relative Humidity	95% noncondensing					

NOTES:
1. OPEN-TO-CLOSED: The delay required to detect an input contact closure switching from open-to-closed.
2. CLOSED-TO-OPEN: The delay required to detect an input contact closure switching from closed-to-open.
3. Contact debounce time.
4. Contact state.
5. The on-board DC-to-DC converter provides three isolated voltages. Each voltage services one block of eight input channels.
6. This is for a 60Hz signal.
7. Common power supplies used for contact wetting degrades channel-to-channel isolation.

MECHANICAL SPECIFICATIONS

Compatible with IEEE-796 (Multibus) specifications
Minimum card spacing: 0.6" (15.2mm)
Board Thickness: 0.062" (1.57mm)
Bus connector: P1: 43/86 pin on 0.156" (3.9mm) centers
P2: auxiliary: 30/60 pin on 0.10" (2.5mm) centers
I/O connectors: P3/P4: 25/50 pin on 0.10" (2.5mm) centers

INSTALLATION

The MP810 series cards are shipped from the factory ready for immediate use. Installation requires only address configuration, inserting the card into an empty slot in the computer and wiring the input connector.

OPERATING INSTRUCTIONS

ADDRESSING

The base address of the MP810 is factory set to F600 hexadecimal. The base address can be changed to any value by installing the appropriate jumpers (see Table I). The board can also be configured to respond to a 20-bit address by installing W69.

Memory inhibit signals (INH1 and INH2) are asserted by the MP810. This allows the board to overlay system ROM and RAM.

TABLE I. Address Jumpers.

ADDRESS	FACTORY SET	INSTALLED FOR 1	INSTALLED FOR 0
ADR2	0	W1	W2
ADR3	0	W3	W4
ADR4	0	W5	W6
ADR5	0	W7	W8
ADR6	0	W9	W10
ADR7	0	W11	W12
ADR8	0	W13	W14
ADR9	1	W15	W16
ADRA	1	W17	W18
ADRB	0	W19	W20
ADRC	1	W21	W22
ADRD	1	W23	W24
ADRE	1	W25	W26
ADRF	1	W27	W28
ADR10	NC	W29	W30
ADR11	NC	W31	W32
ADR12	NC	W33	W34
ADR13	NC	W35	W36
16-bit address	W69 open		
20-bit address	W69 installed		

PROGRAMMING

Data is read in 8-bit bytes. Each bit represents the state of one channel. Table II shows the memory map for the card and relates channel numbers to bit positions. Address bits ADR0 and ADR1 are used to select the data byte. Note that the board has one unused memory location. A logic 0 represents a low voltage or open contact. A logic 1 represents a high voltage or closed contact. Data is acquired through a memory read operation. The example shown is for a single byte operation, however, data from the first 16 channels can be acquired with a 2-byte memory operation.

TABLE II. Memory Map and Channel Position.

ADDRESS	BASE	BASE + 1	BASE + 2	BASE + 3
Factory set (hexadecimal)	F600	F601	F602	F603
Bit 0	Ch 0	Ch 8	Ch 16	*
1	1	9	17	*
2	2	10	18	*
3	3	11	19	*
4	4	12	20	*
5	5	13	21	*
6	6	14	22	*
7	7	15	23	*

* Not used

EXAMPLE:

Read channels 0 through 7

1. Read data
   Command: LDA F600H
   Loads accumulator with data
2. Interpret data
   Assume data is 5CH
   Binary 0 1 0 1 1 1 0 0
   Channel 7 6 5 4 3 2 1 0
   Contacts open (low voltage) on channels 0, 1, 5 and 7
   Contacts closed (high voltage) on channels 2, 3, 4 and 6

ISOLATION

Two methods of isolation are used on the MP810. First, optical couplers provide isolation between signal inputs and the system. Second, an isolated DC/DC converter generates three isolated voltage sources for contact wetting (sensing) on the MP810 and MP810-DB only. Each supply provides power to sense contact closures for a block of eight inputs. These blocks are shown in Table III. Isolation between blocks is 600V. The common supplies degrade channel-to-channel isolation within a block of channels. The DC/DC converters are not present in the MP810-NS, MP810-LV, and MP810-AC. Therefore, these products have channel-to-channel isolation of 300VDC in addition to 600VDC isolation between blocks of channels. This is illustrated in Figure 1.

TABLE III. Isolation Groups.

BLOCK	CHANNEL NUMBER	CONNECTOR	-12V PINS
1	0-7	P3	27, 28, 29, 30
2	8-15	P3	39, 40
		P4	15, 16
3	16-23	P4	47, 48, 49, 50

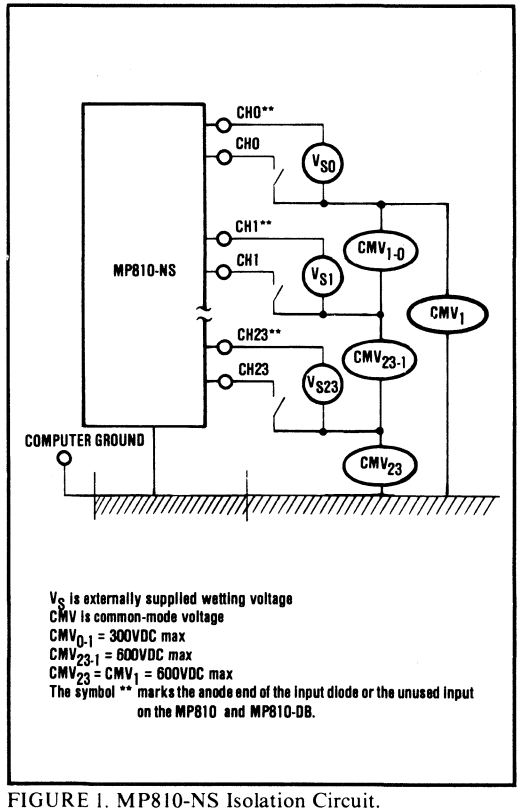

FIGURE 1. MP810-NS Isolation Circuit.

INPUT CIRCUIT

The basic input circuit for the MP810 series is shown in Figure 2. A current of 1mA will assure a logic 1 and a current of less than 0.1mA will assure a logic 0. An input current greater than 1mA for a logic 1 is recommended to improve noise rejection.

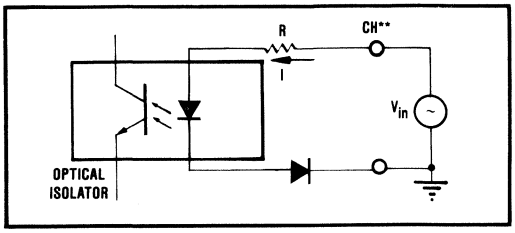

FIGURE 2. Basic Input Circuit.

Dry Contact Inputs (MP810/MP810-DB)

Dry contact (switch) closures can be sensed by the MP810 (MP810-DB) when contacts are connected as shown in Figure 3. The ±12V supplies are generated from the system +12VDC supply via a DC/DC converter. Current in the circuit is determined by the sum of the series resistor and contact resistance. Recommended contact resistance values are shown.

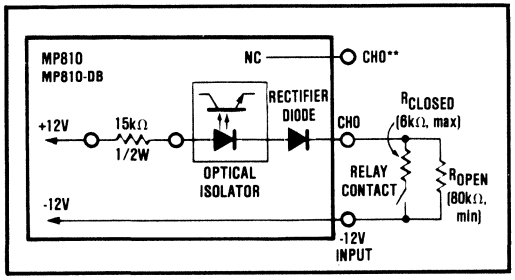

FIGURE 3. MP810, MP810-DB Dry Contact Input Circuit.

Dry Contact Input Debounce (MP810-DB)

The MP810-DB has the same input configuration as the MP810. It differs from the MP810 in that a debounce circuit has been added as shown in Figure 4.

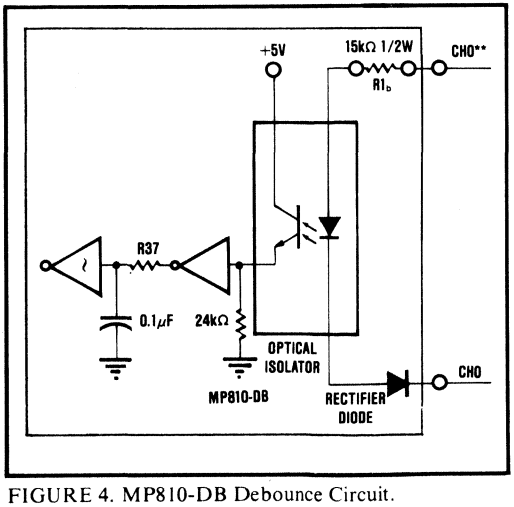

FIGURE 4. MP810-DB Debounce Circuit.

Wet Contact Inputs

The closure of a contact connected in series with an external power supply (wetted contact closures) can be sensed by the MP810-NS or MP810-LV when connected in series with the input as shown in Figure 5. Table IV lists recommended contact resistance values.

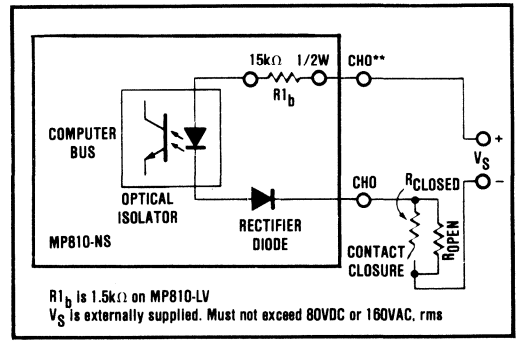

FIGURE 5. MP810-NS, MP810-LV Wet Contact Input.

TABLE IV. Recommended Contact Resistance for MP810-NS.

RCLOSED	at 24V across contacts	6kΩ, max
	at 48V across contacts	30kΩ, max
	at 60V across contacts	58kΩ, max
ROPEN	at 24V across contacts	80kΩ, min
	at 48V across contacts	175kΩ, min
	at 60V across contacts	235kΩ, min

RCLOSED — The impedance of an input contact when closed. RCLOSED specification is the maximum impedance allowed to reliably detect a closure. See Figure 1.

ROPEN - The impedance of an input contact closure when open. ROPEN specification is the lowest impedance allowed to reliably detect an open contact.

NOTE MP810-LV is not rated for these voltages.

TTL Inputs (MP810-LV)

MP810-LV will sense TTL input levels when connected as shown in Figure 6. This circuit uses an open collector gate to sink current through the input circuit.

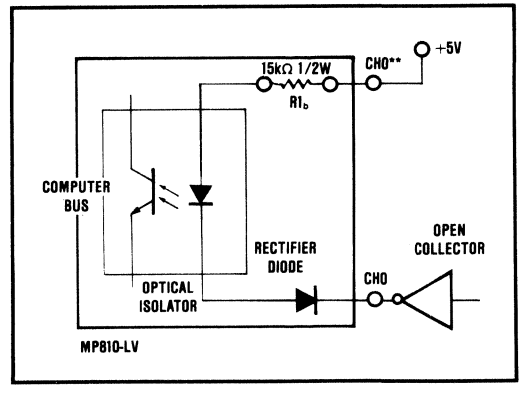

FIGURE 6. MP810-LV TTL Input.

AC Inputs

MP810-AC will sense the presence or absence of an AC signal. This signal is half-wave-rectified by the input diodes. A debounce circuit filters the signal that passes through the optical coupler to maintain a steady state signal when an AC signal is present. Reference Figure 7.

ACCESSORIES

Connector, Input/Output 225OMC

Terminations: For P3 Channels 1-12..... SM50018
For P4 Channels 13-24..... SM50016

Cable, Input/Output SM50037

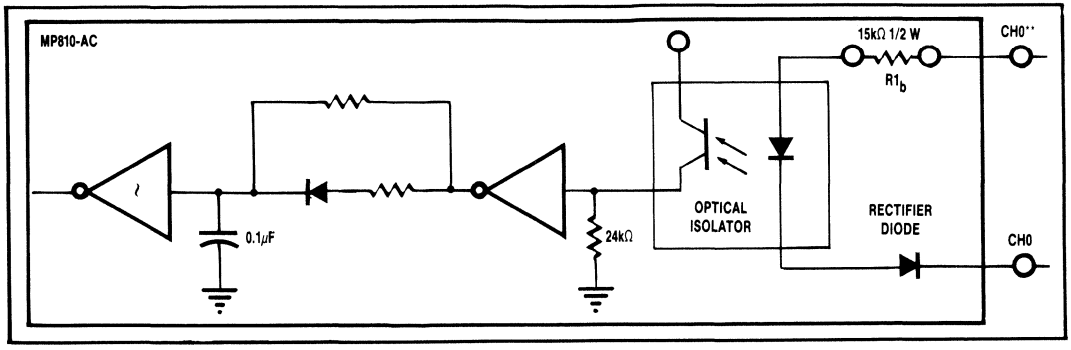

FIGURE 7. MP810-AC Debounce Circuit.

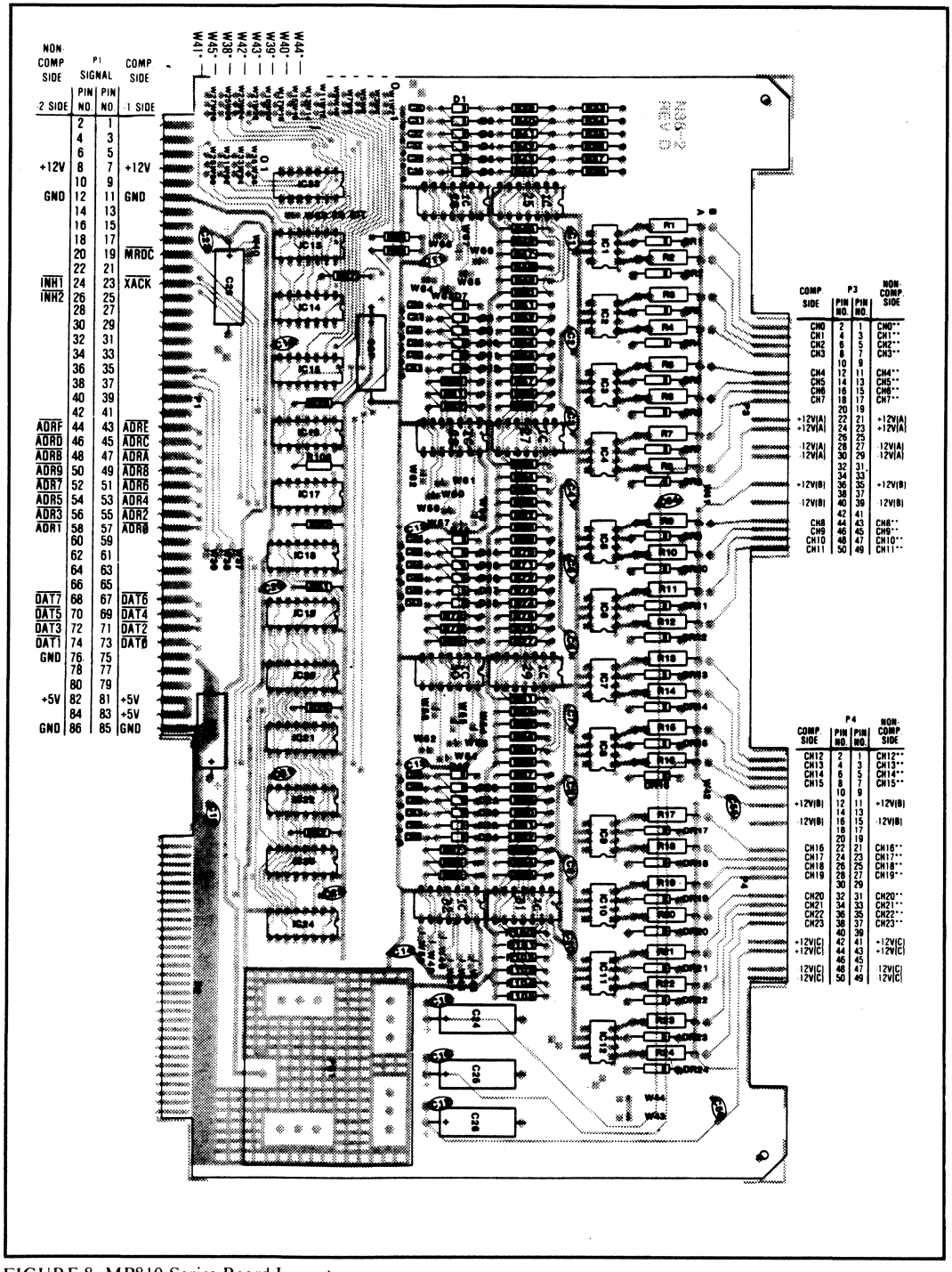

FIGURE 8. MP810 Series Board Layout.

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MP820-05
MP820-15
MP821-05
MP821-15

ADVANCE INFORMATION
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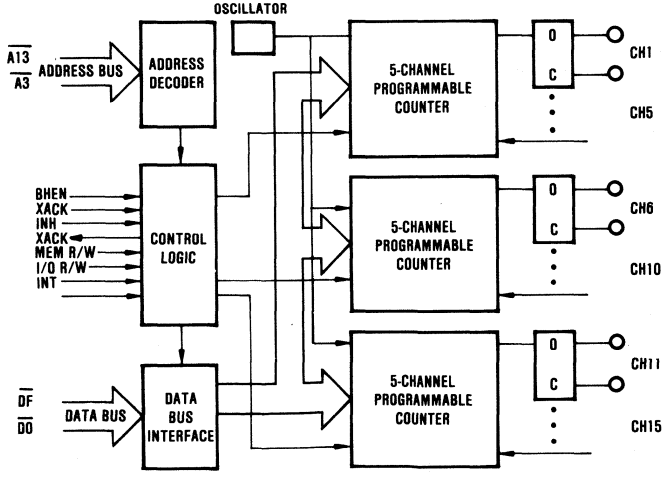
MICROCOMPUTER DIGITAL INPUT SYSTEM

5- or 15-Channel Isolated Pulse Counter/Measurement System Compatible with IEEE-796 (Multibus™)

FEATURES

- 5 OR 15 CHANNELS
- 16-BIT COUNTER
- SINGLE OR DOUBLE PRECISION
- REGISTER TRANSFER
- MEMORY OR I/O MAPPED
- OPTICALLY-ISOLATED INPUTS
- DEBOUNCE
- FREQUENCY (MP821 ONLY)
- PULSE DURATION (MP821 ONLY)
- MULTIBUS™ COMPATIBLE
- 20-BIT ADDRESS BUS
- 16-BIT DATA BUS
- BURNED-IN



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MP830-72

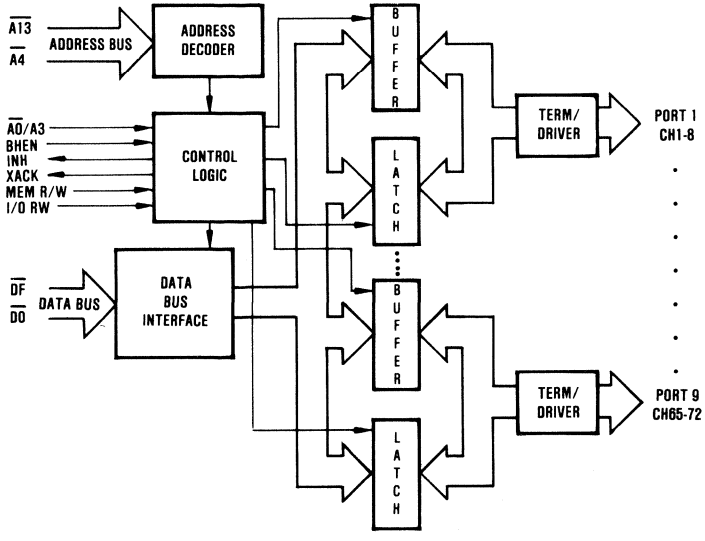
ADVANCE INFORMATION
Subject to Change

MICROCOMPUTER TTL INPUT/OUTPUT SYSTEM

72-Channel TTL Input/Output Systems Compatible with IEEE-796 (Multibus™)

FEATURES

- 72 CHANNELS
- IN/OUT BLOCKS OF 8
- SOCKETED I/O TERMINATIONS
- OUTPUT READ BACK
- LATCHED OUTPUTS
- NO POWER-UP GLITCH
- MEMORY (I/O) MAPPED
- MULTIBUS™ COMPATIBLE
- BURNED-IN



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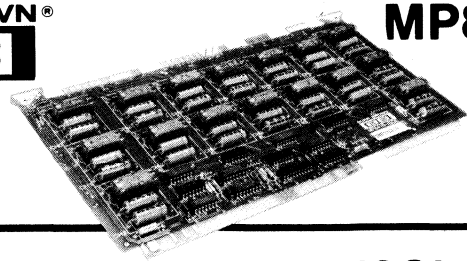
MP8418-ISOE



MICROCOMPUTER ISOLATED ANALOG INPUT EXPANDER FOR MP8418

FEATURES

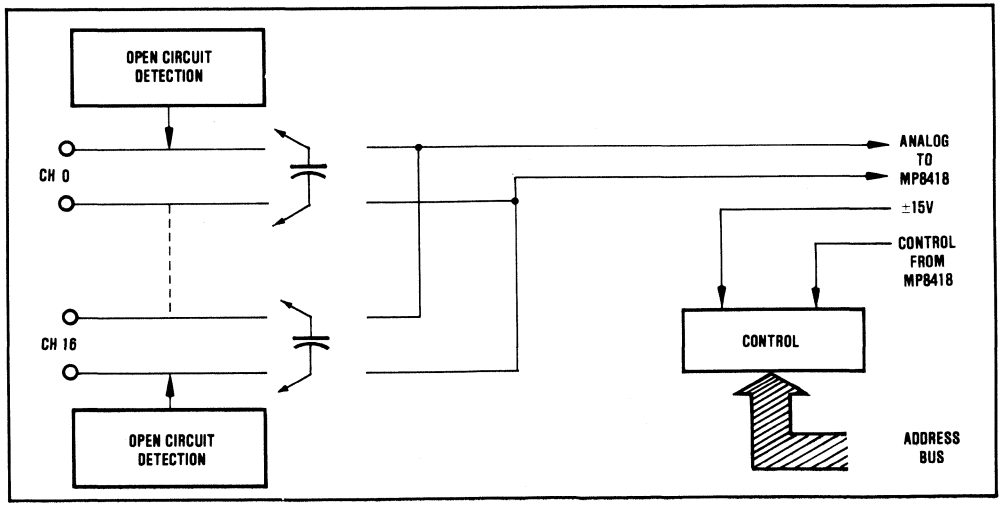
- 400V ISOLATION
- 16 CHANNEL FLYING CAPACITOR MULTIPLEXER
- 8Hz LOW-PASS FILTER
- MULTIBUS™
- LOW THERMAL EMF RELAYS

DESCRIPTION

The MP8418-ISOE expands the analog input capability of the MP8418 family of microcomputer boards from 15 channels to 31, 47 or 63 channels by using one, two or three MP8418-ISOE's. (Note: Only expander channels are isolated. The 15 channels on the MP8418 are standard CMOS multiplexed inputs.) A flying capacitor technique is used to provide 400V input and channel-to-channel isolation. Low thermal EMF relays minimize errors for low level operation. A low-pass input filter on each input provides 60Hz normal-mode rejection.

System interface, signal amplification, and data conversion are provided by the MP8418. Software options and analog signal ranges on the MP8418 are applicable to the MP8418-ISOE. Both boards conform to Intel's Multibus™ specifications.

Multibus™ - Intel Corp.



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THEORY OF OPERATION

Input signals connect to two 50-pin card edge connectors. Every other set of contact fingers is unused to maintain system isolation. Mass termination ribbon cables will have two unused conductors between input channels. This allows mass termination of inputs without degrading isolation. Input connector pinout is shown in the Operating Instructions section. Figure 1 shows the block diagram of the MP8418-ISOE.

A one-pole low-pass filter provides -18dB attenuation at 60Hz. Open circuit detection is provided by a high impedance network that supplies 75nA to the filter capacitors when a channel is left open. The charging current will cause the system to underrange within 4 to 5 seconds at high gain. Time to underrange increases for lower gain settings. At unity gain the capacitor leakage prevents an underrange condition. Dielectric withstanding voltage of the resistors supplying the current is 700V; this maintains system protection at the rated isolation voltage.

Isolation is provided by using a flying capacitor multiplexing technique. Low leakage capacitors and low thermal EMF relays are used to minimize errors for low level operation. Relay contact breakdown is rated at 750Vrms. System isolation is limited to 400VDC or peak by PC board trace spacing.

A 20-pin connector (P5) is mechanically aligned with P4 on the MP8418 to provide easy interface. This connector passes the analog signal (+IN) and return (-IN) to the MP8418. Analog power (±15V) is passed to the expander from the MP8418 along with control signals ADR DEC and EXP . The memory address space in which the expander is located is determined by the MP8418. When the memory space is addressed, the ADR DEC line to the expander goes high. If the expander is being addressed, the EXP line will be low. If a channel on the MP8418 is addressed, EXP will be high.

Connector P6 provides an interface for the external trigger operating mode. This connector sends a trigger pulse to the MP8418 and accepts a BUSY control signal from the MP8418.

Address lines ADR1/ to ADR7/ from the system bus (P1) are latched on board the expander. Address line ADR0/ and MRDC/ are gated with the control lines from the MP8418 to generate a latch pulse. The latch outputs drive two 1-of-8 decoders to enable the appropriate relay.

Control logic gates the control signal from the MP8418 and system bus to do two things. First, a pulse is generated that latches the address data whenever the MP8418 or expander is read by the main CPU and when the LSB of the address is 0 (ADR0/ is HIGH). Second, a timing sequence is started on every other valid read of the expander when the LSB of the address is 0. Gating the LSB of the address allows the CPU to read the MP8418 status and high byte of data without affecting the expander. Timing assumes 0 time delay between conversions. Therefore, it insures that any closed relay is allowed to release, and the newly selected relay will close long enough for the MP8418 to sample the capacitor voltage. This is accomplished by disabling the decoder for 5msec on a valid expander read. At the end of the 7msec time period a second one-shot is started that activates the appropriate relay for 14msec. The timing sequence is disabled on every other read operation and this allows the MP8418 to start a conversion with one read and acquire data with the second.

There are two methods for the MP8418 to sample the capacitor. First, the settling time of the MP8418 can be extended to 18msec. Second, the expander generates a pulse while the capacitor is selected. This pulse can be used to pulse the MP8418 external trigger input. This will start a conversion on the MP8418. In the latter case, the trigger pulse is returned immediately when a channel on the MP8418 is selected. This allows faster conversion times when the expander is not selected.

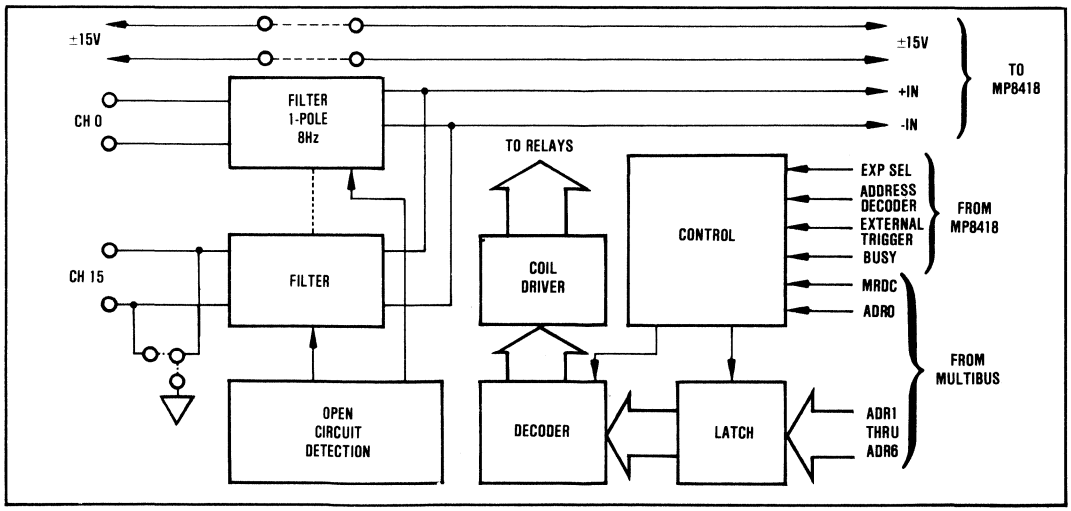


FIGURE 1. MP8418-ISOE Block Diagram.

SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	MP8418-ISOE
Number of Inputs	16 differential
Isolation	400VDC at peak ADC
Filter	8Hz low pass -18dB at 60Hz
Throughput (MP8418)	
Free running	18msec(1)
External trigger	350msec(2) MP8418 17msec MP8418-ISOE
Accuracy(3)	
G = 1	±0.024% of FSR
G = 1024 Software Programmable	±0.10%(4) of FSR
G = 1000 Resistor Programmable	±0.10%(4) of FSR
Power	
+5V ±5%	240mA (system bus
+15V ±5%	0.1A (from MP8418)
-15V ±5%	0.1A (from MP8418)
Environment	
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

NOTES:
1. MP8418 settling time adjusted to 18msec.
2. MP8418 read must occur 10msec after expander read.
3. System accuracy includes MP8418. See MP8418 Data Sheet for amplifier and converter specifications.
4. MP8418 gain and offset adjusted to zero on MP8418-ISOE channel.

MECHANICAL

Compatible with Intellec® MDS and ISBC® - 604/614 card spacing.
Minimum card spacing: 16.2mm (0.6").
Microcomputer bus connector required: 86-pin PC edge connector with 0.156" centers.
Two 50-pin analog edge connectors on board for analog inputs.
Mating connector from Burr-Brown: 2250MC (Viking #VH25/1JN5, solder tab); from 3M: 3415-0001 (Scotchflex).
Two 20-pin analog edge connector on board for MP8418 interface.

Mating cables:

MP8005	single expander, 1" long
SM50123-001	single expander, 9.5" long
SM50123-002	two expanders, 11" long
SM50123-003	three expanders, 12.5" long

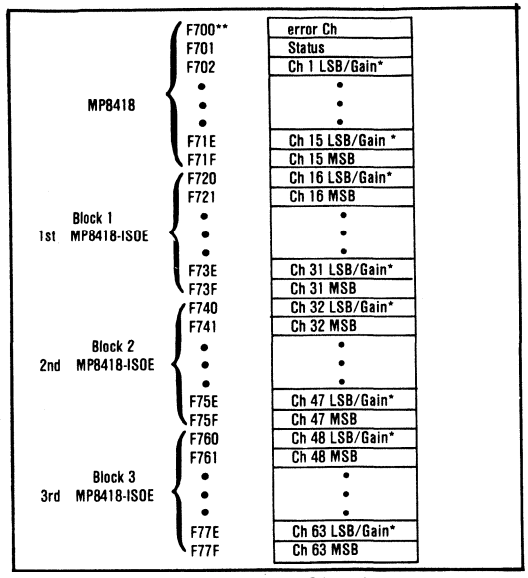
OPERATING INSTRUCTIONS

MEMORY SPACE

The MP8418-ISOE expands the MP8418 input capability in 16-channel blocks. A maximum of three expanders can be connected to a single MP8418. System address decoding is performed on the MP8418 and control signals are passed to the expander. Channel and block decoding are done on the expander. The expander extends the MP8418 address as shown in Figure 2. Jumper configuration is shown in Table I.

OPERATING MODES

MP8418-ISOE can be operated in a free running mode by extending the MP8418 settling time to allow for relay operation, or it can utilize the MP8418 external trigger. Connector P5 on the expander must be connected to P4 on the MP8418 to provide the interface for both modes. See Figure 3.



*Write to these locations stores gain on PGA version.
**Factory set address in hexadecimal.

FIGURE 2. Memory Map.

TABLE I. Jumper Configuration.

BLOCK		1	2*	3
MP8418	Remove	JP42	JP39, 42	JP39, 42
	Install	JP44, 45 JP36, 66	JP44, 45 JP33, 36 JP66, 67	JP44, 45 JP33, 36 JP66, 67
MP8418-ISOE	Remove	JP7, 8	JP6, 8	JP6, 7
	Install	JP6	JP7	JP8

*Note: MP8418 will also respond to Block 3 addresses will return XACK/on bus

Free Running Mode

In this mode the MP8418-ISOE timing is asynchronous to the MP8418 throughput timing. Data appears at the output of the MP8418-ISOE about 16msec after a valid read and remains for 2 to 3msec. Throughput of the MP8418 must be increased to sample data at the appropriate time. This is done by increasing the settling time of the MP8418 to 18msec. Settling time is controlled by C48, R36, R37, and R38 and corresponding one-shot on the MP8418. Remove R36 and R37. Replace C48 with a 1μF capacitor and R38 with a 100kΩ resistor. Use R36 and R37 to adjust the negative pulse at TP5 to 18msec ±1msec.

External Trigger

MP8418-ISOE generates a 1μsec pulse while data is available at the output. This pulse can be used as an external trigger when the MP8418 is set up for external trigger operation. This is done by removing JP17 and

installing JP16 on the MP8418. Also connect P6 on MP8418-ISOE to P5 on MP8418. Connector P5 also provides the analog outputs for analog output versions of the MP8418. The external trigger pulse on the MP8418-ISOE is returned immediately on a valid MP8418 read but delayed for expander reads. An invalid reading will occur if a channel on the MP8418 is read within 10msec of an expander read. The MP8418 settling time does not need to be changed for this mode of operation.

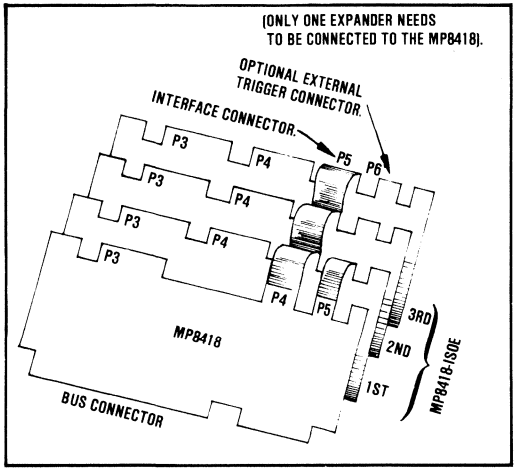


FIGURE 3. Interface Connection.

LOCKOUT

In all operating modes, except the HALT mode, a conversion is started when the CPU reads a low byte of data. When the conversion is complete, the CPU must read the data. A lockout mechanism has been added to prevent the data access operation from starting the timing sequence on the MP8418-ISOE. On power-up or system Reset, a flip-flop is set that enables the MP8418-ISOE timing sequence. The first low byte read (start conversion) starts the timing sequence and changes the state of the flip-flop to disable the timing sequence. The next low byte read will change the state of the flip-flop to enable the timing sequence but not start the sequence. The user should be careful to always follow the start conversion operation with a single low byte data access or else the sequence will be disrupted and invalid data may be received. This feature can be disabled by removing JP9 and installing JP10 for HALT operation.

SAMPLING RATE

Sampling rate is limited by two things. First, the mechanical operation of the relay must be considered. Relay operating time is taken care of by the expander timing with one exception; that is, an MP8418 read following an expander read during external trigger operation (see External Trigger). The second consideration is the time constant of the input filter. There must be enough time between samples on any one channel to allow the capacitor to restore the charge lost during the previous sample. The filter time constant is 25msec. For best results each channel should be given 200msec to recharge before it is resampled. An equivalent circuit for the input is shown in Figure 4. I_B is the amplifier bias current. The -15V source represents the open circuit detection network.

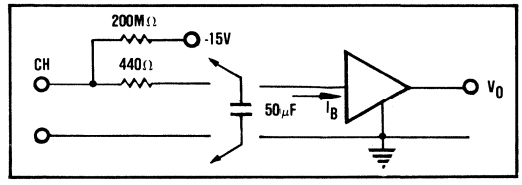


FIGURE 4. Input Equivalent Circuit.

OPEN CIRCUIT DETECTION

An open circuit will cause the system to return a negative full scale value in approximately 10sec at a gain of 1000. The time to reach negative full scale increases as the gain is decreased. At a gain of 2 it takes about two hours for the system to reach negative full scale. At unity gain the system does not reach a negative full scale state due to leakage currents.

SOURCE IMPEDANCE

Source impedance should be less than 100Ω for best performance at high gain. A voltage divider is formed by the source impedance and the open circuit detection network that induces an error of 15R $(R + 2 \times 10^8)$ where R is the source resistance.

FAST AMPLIFIER

The amplifier on the MP8418 and MP8418-AO has a faster response time than does the PGA version. For this reason it is more susceptible to noise caused by digital signals on the control lines to the expander. Best noise performance is obtained by operating in the HALT mode, however, the processor will be disabled for about 18msec. An alternate solution is to decrease the cutoff frequency of the filter at the output of the amplifier on the MP8418. This is done with R31 and C71. A second solution is to add frequency compensation capacitors to the front end amplifiers. Contact the factory for details.

OFFSET ADJUST

The MP8418 and MP8418-ISOE have different input networks as shown in Figure 5. This, in addition to connector cables, causes the offset at high gain of the two analog paths to differ. This can be compensated for by using one of the expander channels to calibrate the system. The error channel on the MP8418 can then be read to provide an adjustment reading for the MP8418 data. This may not be necessary on the PGA version of the MP8418.

UNUSED INPUTS

Unused inputs should be shorted to prevent the filter capacitor from taking on a negative charge from the open circuit detection network. This will improve initial system response as additional channels are added.

ERROR CHANNEL

Jumper JP1 and JP2 allow the user to ground channel 15 on the expander. This channel can then be used as an error reference if desired.

POWER

Analog power (±15V) is supplied to the MP8418-ISOE from the MP8418. These voltages are made available on the input connectors. Only 5mA is available when an AO version of the MP8418 is used. For non-AO versions about 50mA is available, however, this will increase the power consumption of the MP8418.

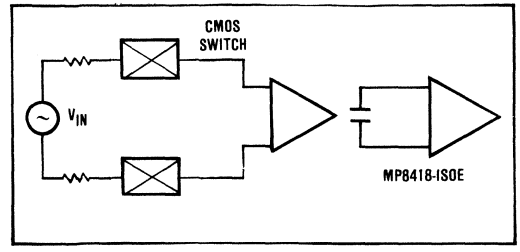


FIGURE 5. Signal Input Network.

CONNECTOR PINOUT

P3

Bottom			Top
+15V	1	2	+15V
GND	3	4	GND
-15V	5	6	-15V
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	NC
RTN7	21	22	CH7
NC	23	24	NC
RTN6	25	26	CH6
NC	27	28	NC
RTN5	29	30	CH5
NC	31	32	NC
RTN4	33	34	CH4
NC	35	36	NC
RTN3	37	38	CH3
NC	39	40	NC
RTN2	41	42	CH2
NC	43	44	NC
RTN1	45	46	CH1
NC	47	48	NC
RTN0	49	50	CH0

P4

Bottom			Top
+15V	1	2	+15V
GND	3	4	GND
-15V	5	6	-15V
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	NC
RTN15	21	22	CH15
NC	23	24	NC
RTN14	25	26	CH14
NC	27	28	NC
RTN13	29	30	CH13
NC	31	32	NC
RTN12	33	34	CH12
NC	35	36	NC
RTN11	37	38	CH11
NC	39	40	NC
RTN10	41	42	CH10
NC	43	44	NC
RTN9	45	46	CH9
NC	47	48	NC
RTN8	49	50	CH8

P5

Bottom			Top
+15V	1	2	+15V
ANA GND	3	4	ANA GND
-15V	5	6	-15V
DIG GND	7	8	ADR DEC
DIG GND	9	10	EXP/
DIG GND	11	12	DIG GND
ANA GND	13	14	ANA GND
ANA GND	15	16	ANA GND
ANA GND	17	18	-IN
ANA GND	19	20	+IN

P6

Bottom			Top
NC	1	2	NC
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
BUSY	19	20	EXT TRIG

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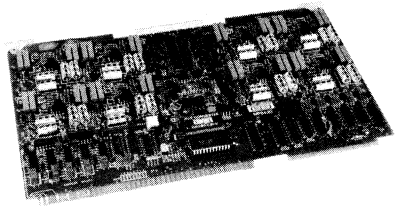


MP8430

MICROCOMPUTER RTD INPUT SYSTEM

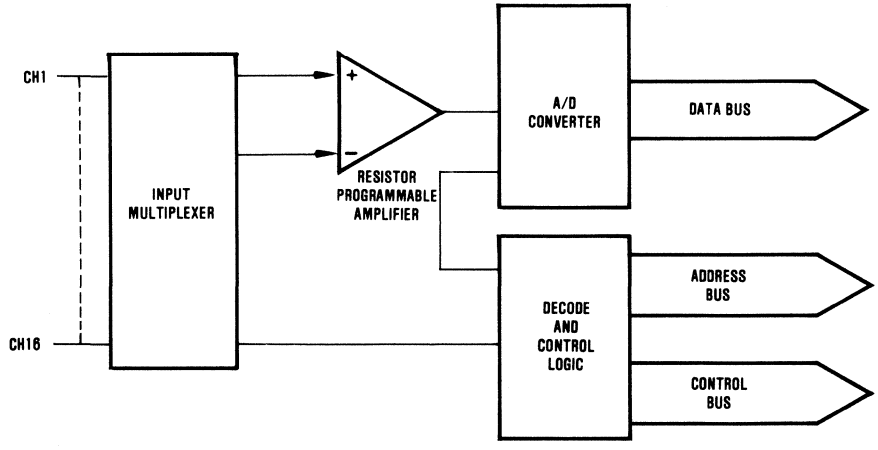
FEATURES

- 16 THREE-WIRE RTD INPUT CHANNELS
- SOLID-STATE MULTIPLEXING
- PROGRAMMABLE GAIN INSTRUMENT AMPLIFIER
- MULTIBUS™ COMPATIBLE (IEEE-796)
- MEMORY OR I/O MAPPED
- LINE LENGTH COMPENSATED

Multibus™-Intel Corporation

DESCRIPTION

The MP8430 is a multiplexed 16-channel RTD input digitizer. Each channel is line length compensated by an exciter circuit which may be calibrated to the device with balance and span adjustments. This circuit produces a voltage, proportional to the temperature of the RTD, which is filtered, multiplexed, amplified, and presented to a 12-bit analog-to-digital converter circuit. The converter in turn is interfaced to the microcomputer bus, thus providing a digital representation of the RTD temperature to the computer.



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SPECIFICATIONS

ELECTRICAL

Typical specifications at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	MP8430
INPUT	
Type	3-wire resistive temperature device (RTD)
Resolution	12-bit (one-part in 4096)
Zero (balance)	
Setting	100Ω
Range (25-turn)	0Ω to 200Ω
Excitation Current	
Setting (nominal)	0.7546mA
Range	0.73mA to 0.78mA
Gains Fixed	x31, x100
Gain Equation	$\frac{R107 + 25k\Omega}{R107}$
(user set gain)	
ADC Input Range	-5VDC to +5VDC
Maximum Line Resistance	4000Ω
(1/2-loop resistance)	
One-Pole Input Filter	0.33Hz
ACCURACY	
System Accuracy at +25°C	±0.10Ω
Temperature Drift	100ppm/°C
THROUGHPUT	
Throughput Time	85μsec
Settling Time	60μsec
Conversion Time	25μsec
BUS STRUCTURE	Multibus™ (IEEE-796)
POWER REQUIREMENTS	
+5VDC, ±5%	0.35 amp
+12VDC, ±5%	0.35 amp
-12VDC, ±5%	0.14 amp
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Storage Temperature	-25°C to +85°C
Relative Humidity	95% noncondensing

INSTALLATION

MP8430 is shipped from the factory ready for use. Installation consists of setting the correct address, plugging the card into any empty slot in the Multibus computer, and wiring the RTD connector.

ADDRESSING

MP8430 may be operated either memory-mapped or I/O-mapped (jumper selected). The board occupies four bytes of address space and can be placed on any four byte boundary. Eight, 12, 16, or 20-bit memory or I/O mapping are selectable.

PROGRAMMING

MP8430 is programmed in either the polled-mode or interrupt-mode, the difference being that the status register must be read in the polled-mode to determine completion of a conversion, whereas the interrupt-mode signals completion of a conversion by setting an interrupt to the processor.

Interrupt-mode is enabled by writing a "1" to bit 'D6' in the Status register (base address + 1). The appropriate interrupt jumper (W31-W38) must also be installed on the board.

A conversion is initiated by writing a channel number to the Control register (base address). The channel number is a hexidecimal 0 through F to select one of 16-channels. During conversion, bit "D7" of the Status register will be a '1'. When the conversion is completed, this bit will return to '0' indicating that valid data is in the data registers.

Data is typically read first from the Data Low register (base address + 2), then from the Data High register (base address + 3). This can be done with a single "LHLD" instruction. Writing a '1' to bit 'D4' of the Status register will clear the interrupt if operating in the interrupt-mode.

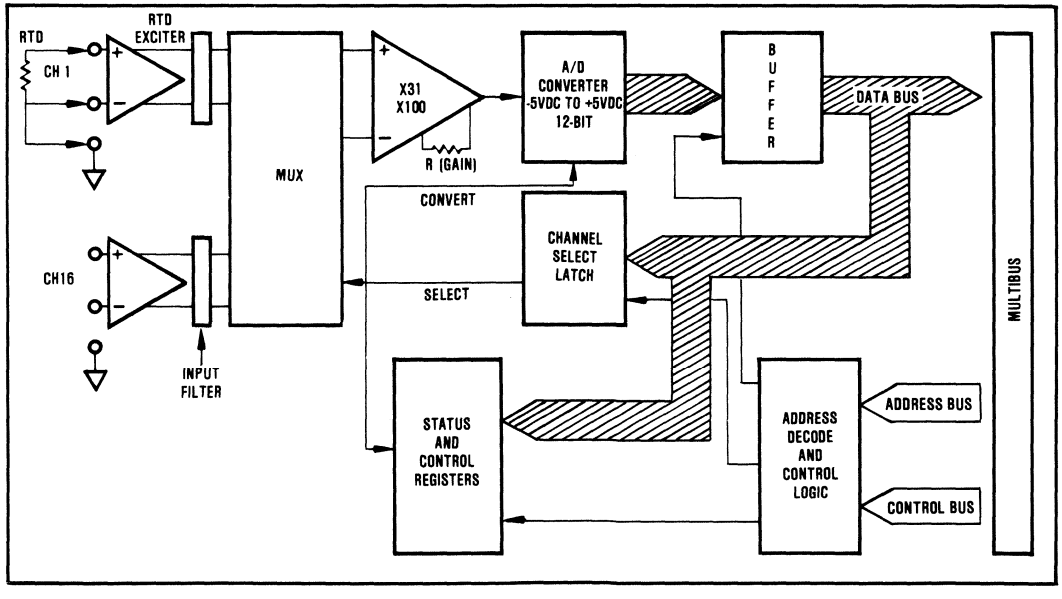

FIGURE 1. Block Diagram.

			D7	D6	D5	D4	D3	D2	D1	D0
BASE ADDRESS	CONTROL	WRITE	X	X	X	X	C3	C2	C1	C0
		READ	0	0	1	1	1	0	0	0
+1	STATUS	WRITE	X	INTE	X	INTC	X	X	X	X
		READ	STAT	INTE	X	INTR	X	X	X	X
+2	DATA LOW	READ	B7	B6	B5	B4	B3	B2	B1	B0
+3	DATA HIGH	READ	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	$\overline{B11}$	B10	B9	B8

1. WRITE TO CONTROL REGISTER - CAUSES CHANNEL (0-15) TO BE CONVERTED.
2. READ FROM CONTROL REGISTER - CARD ID. (always 38H).
3. WRITE TO STATUS REGISTER - SET INTERRUPT ENABLE (D6). HIGH IS ENABLED. CLEAR INTERRUPT (D4). HIGH IS CLEARED.
4. READ FROM STATUS REGISTER - CONVERSION STATUS (D7) HIGH DURING CONVERSION. INTERRUPT ENABLE (D6). HIGH IS ENABLED. INTERRUPT STATUS (D4) HIGH CONVERSION COMPLETED.
5. READ DATA LOW - CONVERTER BITS (B0-B7).
6. READ DATA HIGH - CONVERTER BITS (B8-B11).

FIGURE 2. MP8430 Registers.

CHANNEL	C3	C2	C1	C0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
15	1	1	1	1

FIGURE 3. Channel Selection.

TABLE I. Data Conversion.*

INPUT RESISTANCE		DATA (TWO'S COMPLEMENT)											
X31	X100	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
313.74	166.26	0	1	1	1	1	1	1	1	1	1	1	1
		•	•	•	•	•	•	•	•	•	•	•	•
		•	•	•	•	•	•	•	•	•	•	•	•
100	100	0	0	0	0	0	0	0	0	0	0	0	0
		•	•	•	•	•	•	•	•	•	•	•	•
		•	•	•	•	•	•	•	•	•	•	•	•
N/A	33.74	1	0	0	0	0	0	0	0	0	0	0	0

*FOR 100Ω ZERO ADJUSTED RTD. BIT WEIGHT EQUAL TO 0.03235Ω PER BIT. FACTORY ZERO ADJUSTMENT TO 100Ω.

USER CONFIGURABLE OPTIONS

	BUS WIDTH SELECTION		
		INSTALL	REMOVE
ADDRESS	20-BIT (20B)	W6, W7, W8	
BUS WIDTH	16-BIT (16B)	W7, W8	W6
	12-BIT	W8	W6, W7
	8-BIT		W6, W7, W8

NOTE:
These jumpers are identified as 20B, 16B, and I/O on the silkscreen.

MAPPING SELECTION
MEMORY-MAPPED - Install W28, W29 A Position
I/O-MAPPED - Install W28, W29 B Position

BASE-ADDRESS SELECTION
Install jumpers W10 - W27 in the appropriate '1' or '0' positions.
NOTE: These jumpers are identified as A2-A13 (Hex) on the silkscreen.

GAIN SELECTION
G = 31 Install W3 Position B (factory setting)
G = 100 Install W3 Position A

FIGURE 4. MP8430 Options.

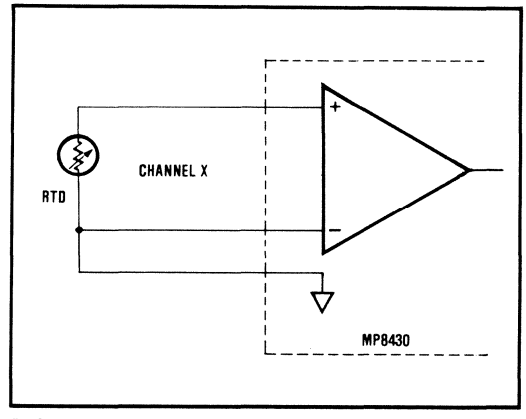

FIGURE 5. Input Connections.

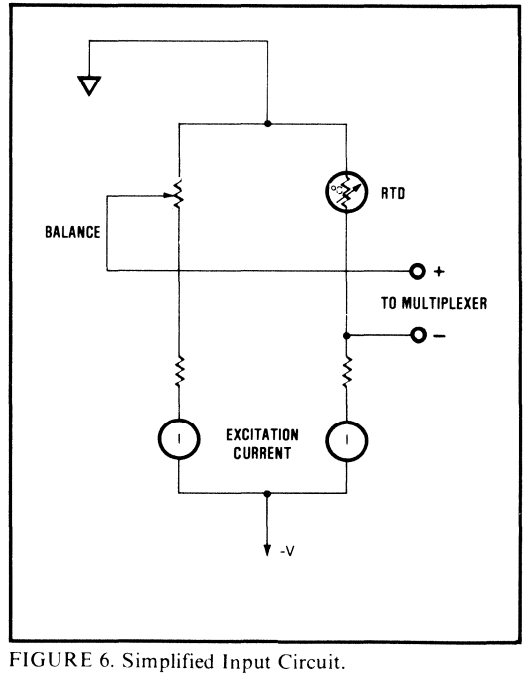

FIGURE 6. Simplified Input Circuit.

CONNECTOR PINOUT

P3 EDGE CONNECTOR			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	GND	2	GND
3	CH16+	4	CH8+
5	CH16-	6	CH8-
7	CH16 GND	8	CH8 GND
9	CH15+	10	CH7+
11	CH15-	12	CH7-
13	CH15 GND	14	CH7 GND
15	CH14+	16	CH6+
17	CH14-	18	CH6-
19	CH14 GND	20	CH6 GND
21	CH13+	22	CH5+
23	CH13-	24	CH5-
25	CH13 GND	26	CH5 GND
27	CH12+	28	CH4+
29	CH12-	30	CH4-
31	CH12 GND	32	CH4 GND
33	CH11+	34	CH3+
35	CH11-	36	CH3-
37	CH11 GND	38	CH3 GND
39	CH10+	40	CH2+-
41	CH10-	42	CH2-
43	CH10 GND	44	CH2 GND
45	CH9+	46	CH1+
47	CH9-	48	CH1-
49	CH9 GND	50	CH1 GND

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MP8450

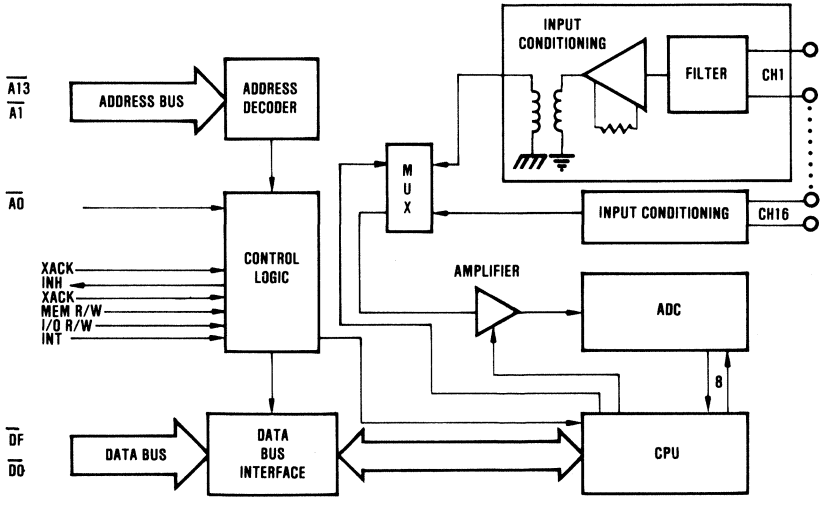
ADVANCE INFORMATION
Subject to Change

MICROCOMPUTER ANALOG INPUT SYSTEMS

16-Channel Analog Input System Compatible with IEEE-796 (Multibus™)

FEATURES

- TRANSFORMER-ISOLATED INPUTS
- 700V ISOLATION
- 1000V ISOLATION WITH COATING
- INPUT FILTER
- OPEN CIRCUIT DETECTION
- RESISTOR-PROGRAMMABLE-GAIN PER CHANNEL
- MEMORY OR I/O MAPPED
- REGISTER TRANSFER OF DATA
- 20-BIT ADDRESSABLE
- BURNED-IN



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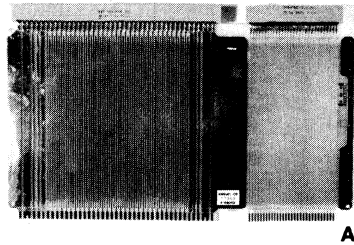

MP8510

ADVANCE INFORMATION
Subject to Change

MULTIBUS™ EXTENDER BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- ALLOWS EASY TESTING OF MULTIBUS CARDS
- RAISES BOARD UNDER TEST 6.9 INCHES

DESCRIPTION

The extender board allows a Multibus user to raise a board being tested above the level of the other boards in the system. The extender board is a standard size Multibus card which contains lines which go directly to the top of the board from the main and auxiliary edge card fingers on the bottom of the board. At the top of the board they are connected to a set of edge connectors to which the user can plug in the board under test.

Heavy duty lines are provided for all power supplies, and one side of the board is a ground plane to minimize noise.

Multibus™ - Intel Corp.

SPECIFICATIONS

PHYSICAL CHARACTERISTICS
Width: 12.00" (30.48cm)
Height: 7.25" (18.42cm)
Depth: 0.4" (1.02cm)
Weight: 10oz (284gm)

ORDERING INFORMATION
Part Number: MP8510
Description: Multibus Extender Board

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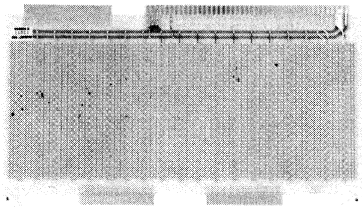

MP8511

ADVANCE INFORMATION
Subject to Change

MULTIBUS™ PROTOTYPING BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- **ALLOWS UP TO 95:16 PIN SOCKETS TO BE WIRE-WRAPPED**
- **+5V AND GROUND BUSSED THROUGHOUT THE BOARD**
- **TWO 50-PIN AUXILIARY CONNECTORS ARE AVAILABLE ON THE TOP OF THE BOARD**

SPECIFICATIONS

BOARD CAPACITY
95 16-pin sockets or their equivalents

PHYSICAL CHARACTERISTICS

Width:	12.00" (30.48cm)
Height:	6.75" (17.15cm)
Depth:	0.25" (0.64cm)
Weight:	6oz (170gm)

ORDERING INFORMATION
Part Number: MP8511
Description: Multibus Prototyping Board

DESCRIPTION

This board allows a user to wire-wrap a prototype circuit for the Multibus. The board is laid out so that sockets with pin spacings of both 0.3" and 0.6" will fit conveniently. Up to 95:16 pin sockets (or an equivalent mix of 14, 16, 18, 20, 24, 28, or 40 pin sockets) will fit on the board at one time. Two 50-pin edge connectors are provided on the top of the board for connections to external devices. Also, holes are provided for wire-wrap pins which will make connections to all main and auxiliary edge collectors.

Power (+5V and ground) is bussed throughout the board to make convenient and short connections to all IC's. The other power supplies are available near the main edge connector for routing to the desired location.

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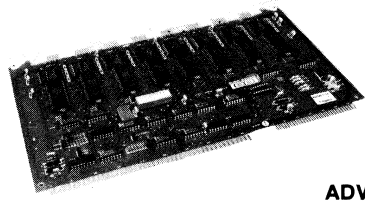

MP8518

ADVANCE INFORMATION
Subject to Change

MULTIBUS™ COMPATIBLE OCTAL SERIAL INTERFACE BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- USES THE SIGNETICS 2651 USART
- FULL 16-BIT DIP-SWITCH ADDRESSING STRAP SELECTABLE
- STRAPS SELECT FULL RANGE OF INTERRUPT CAPABILITIES
- PROGRAMMABLE BAUD RATE FROM 50 TO 19,200 BAUD

SPECIFICATIONS

WORD SIZE
8 bits

ADDRESSING
This board requires 32 I/O ports. The base address for these ports can be on any 32-port boundary. Normally, 16-bit addressing is used for port selection. By changing a strap, however, 8-bit addressing can be selected.

Each USART requires four consecutively addressed ports, and their function is described below.

Address	Input Function	Output Function
0	Receiver data register	Transmitter data register
1	Status register	SYN/DLE registers
2	Mode registers (1/2)	Mode registers (1/2)
3	Command register	Command register

ACCESS TIME
450nsec max

BAUD RATES AVAILABLE
50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200

INTERRUPT SOURCES
Any transmitter empty condition or receiver full condition can trigger an interrupt. Independent straps allow all transmitter interrupts or all receiver interrupts to be disabled. All interrupts from the board go to any one of the eight vectored interrupt lines on the Multibus.

RS-232 SPECIFICATIONS
The drivers and receivers used on the board are the 1488 and 1489 type. This provides a compatible interface for the following lines: TxD, RxD, DTR, RTS, CTS, and DSR.

INTERFACE
All signals meet the IEEE Multibus proposed specification. IEEE 796 Bus Compliance: Slave D8 I16 VO.

PHYSICAL CHARACTERISTICS
Width: 12.00" 30.48cm)
Height: 6.75" (17.15cm)
Depth: 0.5" (1.27cm)
Weight: 10oz (284gm)

ENVIRONMENTAL CHARACTERISTICS
V_{CC} = +5V ±5%
V_{DD} = +12V ±5%
V_{BB} = -12V ±5%
I_{CC} = 1.1A typ, 1.9A max
I_{DD} = 0.1A typ, 0.2A max
I_{BB} = 0.1A typ, 0.2A max

ORDERING INFORMATION
Part Number: MP8518
Description: Multibus Octal Serial Interface Board

DESCRIPTION

This board allows up to eight EIA RS-232 interfaces to be hooked to any Multibus system. Each interface is controlled by a USART which has an on-chip baud rate generator. This enables the user to set each USART at a different speed. Available baud rates range from 50 to 19,200 baud. This board requires 32 I/O ports, and the base address can be set to any multiple of 32 ports.

The I/O addressing on the board can be 8-bit or 16-bit, determined by a strap selection.

The USART used is the Signetics 2651. The user can determine by strap selection various combinations of interrupt servicing. Any receiver full or transmitter empty conditions can be used to generate an interrupt. These interrupts can be disabled by programming the USART accordingly.

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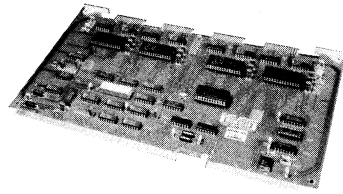

MP8519

ADVANCE INFORMATION
Subject to Change

MULTIBUS™ COMPATIBLE QUAD SERIAL INTERFACE BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- CONTAINS FOUR RS-232 INTERFACES, THREE INTERVAL TIMERS
- USES THE 8251 USART
- FULL 16-BIT DIP-SWITCH ADDRESSING STRAP SELECTABLE
- STRAPS SELECT FULL RANGE OF INTERRUPT CAPABILITIES
- PROGRAMMABLE 75 TO 19,200 BAUD

SPECIFICATIONS

WORD SIZE
8 bits

ACCESS TIME
500nsec max

BAUD RATES PROGRAMMABLE
75, 150, 300, 600, 1200, 2400, 4800, 9600, and 19,200

INTERRUPT SOURCES
All interrupt sources on the board are combined to trigger an interrupt on any of the eight vectored interrupt lines of the Multibus. Straps for each USART determine whether receiver or transmitter interrupts can come from that chip.

ADDRESSING
This board requires 16 I/O ports, and the base address for these ports can be on any 16-port boundary. Full 16-bit dip-switch I/O addressing is a strap-selectable option.

The first eight ports on the board are divided between the USARTs. Each USART gets two consecutive ports, and their functions are as follows:

Address	Input Function	Output Function
0	Receiver holding register	Transmit holding register
1	Status register	Command register

The interval timer uses the next four ports in the following manner:

Address	Input Function	Output Function
8	Read counter 0	Load counter 0
9	Read counter 1	Load counter 1
10	Read counter 2	Load counter 2
11	No-operation	Write control word

RS-232 SPECIFICATIONS
The drivers and receivers used on the board are the 1488 and 1489 type. This provides a compatible interface for the following lines: TxD, RxD, DSR, CTS, DTR and RTS.

INTERFACE
All signals meet the IEEE Multibus proposed specification. IEEE 796 Bus Compliance: Slave D8 I16 VO.

PHYSICAL CHARACTERISTICS
Width: 12.00" 30.48cm)
Height: 6.75" (17.15cm)
Depth: 0.5" (1.27cm)
Weight: 10oz (284gm)

ELECTRICAL CHARACTERISTICS
V_{CC} = +5V ±5%
V_{DD} = +12V ±5%
V_{BB} = -12V ±5%
I_{CC} = 0.85A typ, 1.0A max
I_{DD} = 0.05A typ, 0.1A max
I_{BB} = 0.05A typ, 0.1A max

ORDERING INFORMATION
Part Number: MP8519
Description: Multibus Quad Serial Interface Board

DESCRIPTION

This board allows up to four RS-232 interfaces to be hooked to any Multibus system. The board uses four 8251 USARTs to accomplish parallel-to-serial conversion. Also, the board has three interval timers to control the baud rate of each USART. Since there are only three timers, two of the USARTs must have their baud rate clocks tied together.

Baud rates and specifications for the data transmission are totally programmable by the host computer. This allows the utmost in flexibility of system design. This board uses 16 I/O ports, and is addressable on any 16-port boundary in the Multibus I/O arrangement. The full 16-bit I/O address bus can be used to determine the addressing of the board if desired. This feature can be optionally-disabled.

Straps for each USART can enable interrupts at the end of character transmission or reception.

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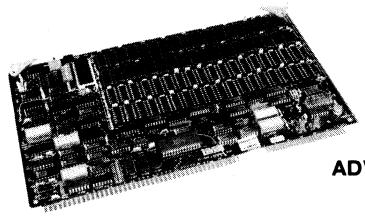

MP8520

ADVANCE INFORMATION
Subject to Change

MULTIBUS™-COMPATIBLE 32K-128K DYNAMIC RAM BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- **DYNAMIC RAM—Low Power Consumption**
- **330nsec ACCESS TIME, 450nsec CYCLE TIME**
- **PARITY CHECKING IS A STANDARD FEATURE**
- **DECODES FULL 24-BIT ADDRESS BUS**
- **PARITY I/O PORT WITH 8- OR 16-BIT ADDRESSING**

SPECIFICATIONS

WORD SIZE
8 or 16 bits, determined by the Multibus BHEN line

MEMORY SIZE
32,768 bytes (32K board) - standard as shipped from Burr-Brown
65,536 bytes (64K board) } user-supplied RAM
98,304 bytes (96K board) }
131,072 bytes (128K board) }

ACCESS TIME
330nsec max

CYCLE TIME
450nsec max

ADDRESS SELECTION
Dip-switch addressing for each 64K section to reside on any 64K memory boundary in the 16 megabyte address space. Four switches for each of the two sections allow enabling of any 16K within the addressed space.

16-bit dip-switch address selection for the I/O port is used, with A8-A15 optionally disconnected.

INTERFACE
All signals meet the IEEE Multibus proposed specification. IEEE 796 Bus Compliance: Slave D16 M24 I16.

PHYSICAL CHARACTERISTICS
Width: 12.00" (30.48cm)
Height: 6.75" (17.15cm)
Depth: 0.5" (1.27cm)
Weight: 19oz (539gm)

ELECTRICAL CHARACTERISTICS
V_{CC} = +5V ±5%
V_{DD} = +12V ±5%
V_{BB} = -12V ±5%
I_{CC} = 1.7A typ, 2.3A max
I_{DD} = 0.71A typ, 0.71A max
I_{BB} = 0.01A typ, 0.01A max

ENVIRONMENTAL CHARACTERISTICS
Operating Temperature: 0°C to +55°C
Relative Humidity: 0 to 90% (noncondensing)

ORDERING INFORMATION
Part Number: MP8520
Description: Multibus Dynamic RAM Board

DESCRIPTION

This board allows Multibus users to add 32K, 64K, 96K, or 128K of RAM to their systems. A standard feature of the board is parity checking, which will generate an interrupt if any single bit memory error occurs. The CPU can then read an input port to determine which row of RAMs had the error. Also, four LEDs on the top of the board indicate the check condition and determine which row of memory chips failed. This allows fast replacement in the event of a failure. Writing to the corresponding output port clears the parity error.

The board is completely Multibus-compatible and runs at a maximum access time of 330nsec. All lines into the board are buffered, and the data out lines can take the form of 8 or 16 bits, depending on the BHEN line of the Multibus. This allows the board to work without changes in any 8- or 16-bit system.

An on-board -5V regulator provides the negative supply needed by the RAM chips. This eliminates the requirement for a -5V input to the board.

The board decodes the full 24-bit address bus, allowing the system-wide memory address capacity of 16 megabytes. The board is divided into two 64K sections for addressing. Each section can be addressed on a 64K memory boundary. Additionally, straps allow the user to enable each 16K segment within these sections.

Refresh on the board is designed to cause no extra wait-states in normal operation. This is accomplished by doing refreshes (when required) after normal bus cycles. If no read or write memory cycles are present on the bus for a predetermined length of time, the board starts refreshing on its own.

The board undergoes extensive testing and burn-in prior to shipment. It also makes extensive use of LSI controller chips designed for dynamic RAM applications to increase reliability.

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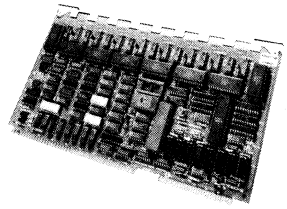

MP8525

ADVANCE INFORMATION
Subject to Change

MULTIBUS™-COMPATIBLE INTELLIGENT OCTAL SERIAL INTERFACE BOARD FOR MICROCOMPUTER ANALOG I/O SYSTEMS

FEATURES

- **CONNECTS EIGHT RS-232 PORTS TO ANY MULTIBUS SYSTEM**
- **USES SIGNETICS 2651 USART AND 2650 MICROPROCESSOR**
- **ON-BOARD PROCESSOR HANDLES ALL I/O INTERRUPTS, FREEING TIME FOR THE HOST PROCESSOR**
- **16K OF DUAL-PORT RAM USED AS BUFFERS FOR DATA IN AND OUT**

DESCRIPTION

This board allows up to eight EIA RS-232 interfaces to be attached to any Multibus system. Each interface is controlled by a USART which has an on-chip baud rate generator. This enables the system to set each USART at a different speed. Available baud rates range from 50 to 19,200 baud.

The USARTs are controlled by an on-board 2650 microprocessor. This processor handles all interrupts from the devices, and is responsible for buffering data to and from each port. Up to 4K bytes of PROM can be on-board to control the 2650. The standard program included with the board (described below) takes only part of one 2K PROM.

16K of dual-port RAM is on the board, to which the 2650 and the Multibus have access. The host processor places data into this RAM which is to be sent out, and the 2650 reads it and sends it to the proper USART. Likewise, on incoming data, the 2650 takes the data and places it into the buffer RAM where the host processor can read it.

Since the board is controlled by a microprocessor chip, its function is totally programmable. A standard terminal driver routine is provided with the board, as described below.

TERMINAL DRIVER ROUTINE

Since the board is controlled by a microprocessor, a driver program must be in the board in order for it to function. A terminal driver routine is included with the standard board, and its function is described below.

Each of the eight ports on the board are allocated 2K of memory in the dual-port RAM. All data associated with any particular port is stored in its associated 2K memory block. This 2K block for each port is divided in the following way:

Offset	Length	Description
H000	1920	Output buffer (to device)
H780	64	Input buffer (from device)
H7E0	1	Status
H7E2	1	Input byte
H7E4	2	Offset of byte after last character (outputs)
H7E6	2	Mode control bytes

The output buffer is where the host computer places the data to be sent to the device. Up to 1920 bytes can be placed in the buffer for transmission. The input buffer is where the 2650 stores input characters from the device. This buffer is normally never accessed by the host computer, since it gets its bytes from a fixed location (see below). The status byte has its least significant bit set if the output buffer is empty (and the host processor can fill it with new data), and the next most significant bit set if the input byte holds a new character. The input byte is where the host computer always reads characters sent from the device. The 2650 takes characters from the input buffer (in the order that they are received) and places them into the input byte location. The offset bytes are loaded by the host computer to indicate the length of

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the output buffer. If the host loaded the output buffer with 26 chararacters to be sent (at offsets 0-25 in the output buffer), it would load this word with the value of 26, indicating the offset of the first byte after the data to be sent. The mode control bytes are used when each port is first started to set the baud rate, number of stop bits, etc.

There is one I/O port on the board which is used to tell the 2650 processor that either the host processor has filled the output buffer or that it took the character from the Input Byte, and the 2650 can now put the next character (if any) into that byte. This I/O port can be set to any address on the bus, and its data bits are used in the following manner:

Bit	Function
7	1 = Input, 0 = Output
6-4	Port Number (0-7)
3	1 = Interrupts On, 0 = Off
2-0	Interrupt Level (0-7)

When this address is written for the first time for each port number (0-7), it indicates to the 2650 that it should set up the USART according to the mode control bytes in the common memory. These mode control bytes have the following format:

Even Byte:

Bit 7	Bit 6	Number of Stop Bits
0	0	Invalid
0	1	1
1	0	1.5
1	1	2

Bit 5 = 1 Parity Enabled
Bit 5 = 0 Parity Disabled

Bit 4 = 1 Parity Even
Bit 4 = 0 Parity Odd

Bit 3	Bit 2	Length of Characters
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

Bit 1, Bit 0 = 0

Odd Byte:

Bit 7 = 1 If Auto-Baud Setup
Bit 7 = 0 if Baud Rate as Below

Bit 6 through Bit 4 = 0

Bit 3 through Bit 0 (hex):

0	50 baud
1	75 baud
2	110 baud
3	134.5 baud
4	150 baud
5	300 baud
6	600 baud
7	1200 baud
8	1800 baud
9	2000 baud
A	2400 baud
B	3600 baud
C	4800 baud
D	7200 baud
E	9600 baud
F	19,200 baud

As can be seen, the odd mode control byte can instruct the board to set up the baud rate for the port automatically. The 2650 then starts at 19,200 baud, and waits for a Carriage Return code (HOD) to be received. If it is not received at one baud rate, the next lower baud rate is then tried. Therefore, the device must send a number of Carriage Return codes at power-up in order for the baud rate to be locked in.

After the output port has been written the first time for each USART, the mode has been setup for that port. All further writes to the output port for the USART will be considered command words (the mode cannot be changed unless the board is reset).

Command words are of two types: input and output. When bit 7 of the word is 1, the word is interpreted as an input command. When it is 0, it is an output command.

The input command word tells the 2650 that the host computer has taken the input byte from offset H7E2, and that the 2650 can place the next input byte into that location, if there is one. If no more input characters are available, then the status bit for input is cleared. The interrupt bits of the command word are used to tell what should be done when a new character is moved to the input byte location. If bit 3 is 1, an interrupt will be generated on the specified Multibus vectored interrupt line. If bit 3 is 0, then no interrupt will be generated, and the host computer will have to poll the status location to see if a character is waiting.

Sending an output command word tells the 2650 that the output buffer has been loaded with up to 1920 characters, and that the offset for the byte after the last character has been stored (so the 2650 can tell the length of the block). The 2650 will then start sending the characters out to the proper port. The interrupt bits in this case tell the 2650 what to do when all of the characters in the buffer have been sent.

As noted previously, since the board is controlled by a general-purpose microprocessor, the function of the board is totally programmable. The terminal driver routine provided with the standard board is a convenient way of showing the capabilities of the board, but in no way shows a limit to the board's abilities.

SPECIFICATIONS

WORD SIZE
8 bits. All accesses to the dual-port RAM must be done in 8-bit mode.

ADDRESSING
This board has one output port. It can be addressed using full 16-bit I/O addressing. By changing a strap, only 8-bit I/O addressing is used.

16K of dual-port RAM is on the board, and it can be set to start on any 16K boundary in the system's 16-megabyte address space.

ACCESS TIME
450nsec to 900nsec, depending on whether the dual-port RAM is being refreshed or accessed by the 2650 at the beginning of the cycle.

BAUD RATES AVAILABLE
50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, and 19,200.

INTERRUPT SOURCES
Each port has independent interrupt settings for both Input Character Ready and Output Buffer Empty conditions. Each of the 16 different interrupt sources can specify the Multibus vectored interrupt level (0-7), as well as whether an interrupt should be generated at all (if the board is running in polled mode).

RS-232 SPECIFICATIONS

The drivers and receivers used on the board are the 1488 and 1489 type. This provides a compatible interface for the following lines: T x D, R x D, DTR, RTS, CTS, and DSR.

BUS INTERFACE

All signals meet the IEEE Multibus proposed specification. 796 Bus Compliance: Slave D8 M24 I16VO.

PHYSICAL CHARACTERISTICS

Width: 12.00" (30.48cm)

Height: 6.75" (17.15cm)

Depth: 0.5" (1.27cm)

Weight: 14oz (397gm)

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%

V_{DD} = +12V ±5%

V_{BB} = -12V ±5%

I_{CC} = 2.7A typ, 3.9A max

I_{DD} = 0.2A typ, 0.3A max

I_{BB} = 0.1A typ, 0.2A max

ENVIRONMENTAL CHARACTERISTICS

Operating Temperature: 0°C to +55°C

Relative Humidity: 0 to 90% (noncondensing)

ORDERING INFORMATION

Part Number: MP8525

Description: Multibus Intelligent I/O Board

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